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Editor: E. G. Evans Assistant Editor: M. J. Prescott
Central Technical Services, Mullard Limited, New Road, Mitcham,
Surrey, CR4 4XY. Telephone: 01-648 3471. Telex 22194

Mullard Limited, Mullard House, Torrington Place, London, WC1E 7HD
Telephone: 01-580 6633 Telex: 264341

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F.M. radio front-end with improved large signal handling performance

J. S. Malcolm
Mullard Central Application Laboratory

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This article describes the design of an f.m. radio front-end to give improved reception of a weak signal in the presence of strong interfering signals. Performance measurements are given, and compared with those of a conventional front-end.

INTRODUCTION

As a result of the increasing utilisation of Band II for local and commercial f.m. broadcasting, the ability of an f.m. tuner to receive a weak wanted signal in the presence of strong interfering signals has become a most important performance criterion.

This article summarises the interference effects which can occur in an f.m. tuner subjected to large interfering signals, and describes the design of a front-end having improved large-signal handling performance. The front-end uses a bipolar transistor type BF324 as r.f. amplifier and a low-cost field effect transistor type BF245C as mixer. The resonant circuits are tuned by variable capacitance diodes type BB110.

INTERFERENCE EFFECTS IN F.M. TUNERS

Interference with the reception of an f.m. signal may be caused in a tuner front-end by the four effects described below. Appendix 1 demonstrates the first three of these by analysis of the performance of a non-linear transfer function to which four signals are applied: the wanted signal, the local oscillator signal, an unwanted f.m. signal and (to demonstrate cross-modulation) single-sideband amplitude-modulation of the unwanted signal.

Spurious responses

The reception of a wanted signal may be degraded by an interfering signal at a frequency to which the tuner is simultaneously responsive. The interfering signal frequencies which give rise to a spurious response are the intermediate frequency, the image frequency and the repeat spot frequency. The repeat spot response is generally the most serious source of interference, and its suppression is an important measure of front-end performance.

Intermodulation

When two or more interfering signals are combined in a device with a non-linear transfer characteristic, they may interact to produce a resultant signal at the wanted frequency. This intermodulation may occur in both the r.f. and the mixer stages, and determines the maximum level of interfering signal which may be tolerated.

Cross-modulation

When only pure frequency-modulated signals are present there can be no transfer of modulation from an interfering signal to a wanted signal as a result of transfer function non-linearities, because cross-modulation can only occur if the interfering signal has amplitude variations. Nevertheless, some interfering signals will be amplitude-modulated, and f.m. signals may acquire a.m. components either because of multi-path reception or because of their location on the slope of the tuner r.f. bandpass response, so that the wanted signal may have interfering amplitude-modulation superimposed on it as a result of cross-modulation. The a.m. components of the wanted signal will be substantially suppressed by the limiter and detector stages of the i.f. amplifier; cross-modulation is not, therefore, a primary cause of interference in f.m. front-ends. However, Appendix 1 shows that cross-modulation and intermodulation are related effects, both arising from the same order of non-linearity in a power series expansion of the transfer characteristic. Consequently cross-modulation may be used to characterise the devices used in an f.m. front-end if it is more convenient to measure cross-modulation than intermodulation.

Oscillator pulling

Variations in the amplitude of a large signal will cause impedance variations in the mixer, which can in turn influence the local oscillator frequency. This pulling of the oscillator converts unwanted amplitude-modulation to frequency-modulation of the wanted carrier.

Design criteria

It is anticipated that f.m. tuners may be subjected to signal levels as high as 100mV e.m.f. (75Ω) but as the exact signal conditions cannot be specified, quantitative design criteria cannot be established. The design of an f.m. front-end to have good large-signal handling ability therefore requires that all the interference phenomena, listed above, be minimised.

FRONT-END DESIGN

The circuit diagram of the complete front-end, using the BF324 as an r.f. amplifier and the BF245C as a mixer, is shown in Fig. 1, together with a components list and coil-winding data.

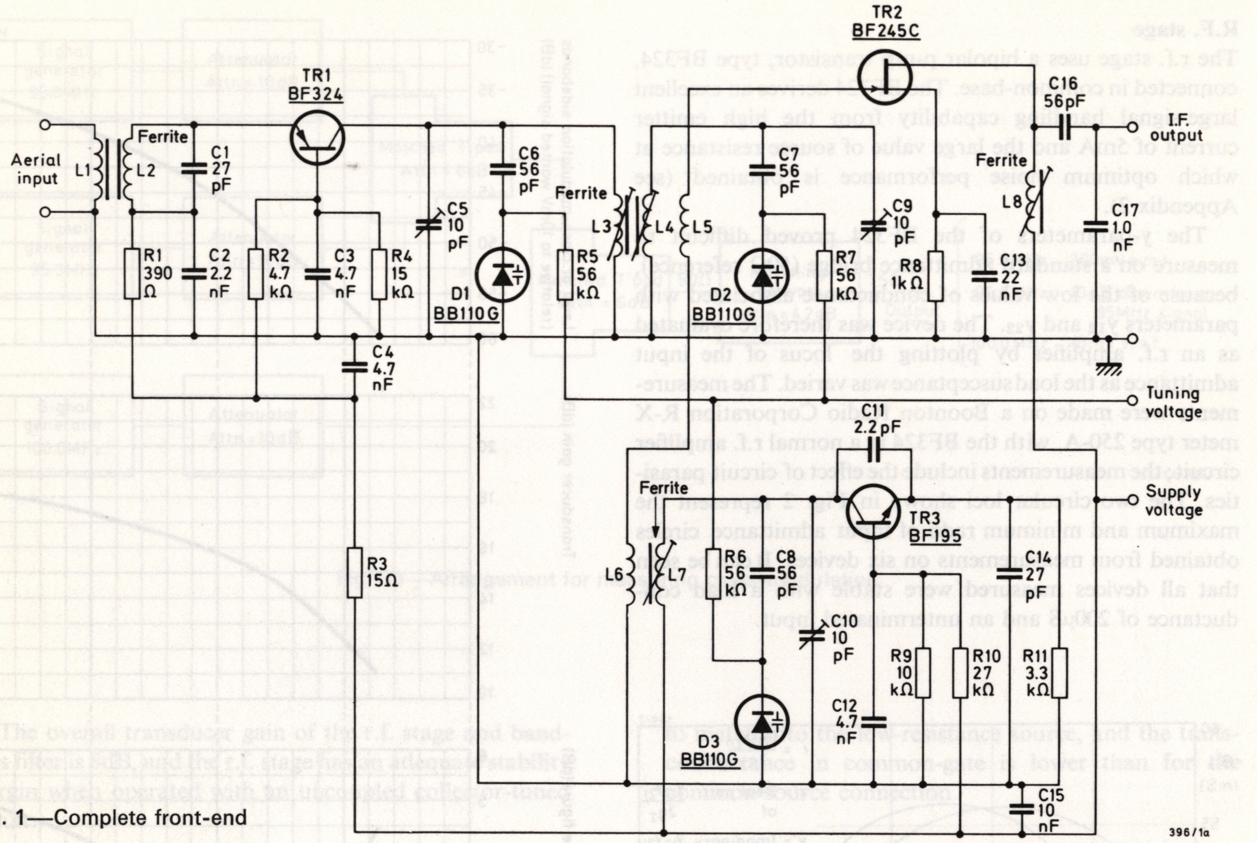

Fig. 1—Complete front-end

COMPONENTS LIST

Transistors

TR$_1$	BF324
TR$_2$	BF245C
TR$_3$	BF195

Diodes

D$_1$	BB110G
D$_2$	BB110G
D$_3$	BB110G

Resistors

All resistors CR25 series, 0·33W, tolerance ±5%

R$_1$	390Ω
R$_2$	4·7kΩ
R$_3$	15Ω
R$_4$	15kΩ
R$_5$	56kΩ
R$_6$	56kΩ
R$_7$	56kΩ
R$_8$	1kΩ
R$_9$	10kΩ
R$_{10}$	27kΩ
R$_{11}$	3·3kΩ

Capacitors

C$_1$	27pF	Miniature ceramic	632 34279
C$_2$	2·2nF	Metallised ceramic	629 02222
C$_3$	4·7nF	Metallised ceramic	629 02472
C$_4$	4·7nF	Metallised ceramic	629 02472
C$_5$	10pF	Film trimmer	809 09002
C$_6$	56pF	Miniature ceramic	632 34569
C$_7$	56pF	Miniature ceramic	632 34569
C$_8$	56pF	Miniature ceramic	632 34569
C$_9$	10pF	Film trimmer	809 09002
C$_{10}$	10pF	Film trimmer	809 09002
C$_{11}$	2·2pF	Miniature ceramic	632 09228
C$_{12}$	4·7nF	Metallised ceramic	629 02472
C$_{13}$	22nF	Metallised ceramic	629 02223
C$_{14}$	27pF	Miniature ceramic	632 34279
C$_{15}$	10nF	Metallised ceramic	629 02103
C$_{16}$	56pF	Miniature ceramic	632 34569
C$_{17}$	1·0nF	Metallised ceramic	629 02102

Inductors

L$_1$, L$_2$	4 and 2½ turns respectively, 28 swg t.n.a., bifilar wound on 5mm diameter former with core.
L$_3$, L$_4$	5 turns, 24 swg en.cu., spaced 1 diameter, on 5mm diameter former with core.
L$_5$	3 turns, 28 swg t.n.a., bifilar wound with L$_4$.
L$_6$	1 turn, 28 swg t.n.a., coupled to L$_7$.
L$_7$	5½ turns, 24 swg en. cu., spaced 1 diameter, on 5mm diameter former with core.
L$_8$	20 turns 3×46 swg litz, wound on 7×7mm coil assembly.

R.F. stage

The r.f. stage uses a bipolar p-n-p transistor, type BF324, connected in common-base. The BF324 derives an excellent large-signal handling capability from the high emitter current of 5mA and the large value of source resistance at which optimum noise performance is obtained (see Appendix 2).

The y-parameters of the BF324 proved difficult to measure on a standard admittance bridge (50Ω reference), because of the low values of conductance associated with parameters y_{12} and y_{22}. The device was therefore evaluated as an r.f. amplifier by plotting the locus of the input admittance as the load susceptance was varied. The measurements were made on a Boonton Radio Corporation R-X meter type 250-A, with the BF324 in a normal r.f. amplifier circuit; the measurements include the effect of circuit parasitics. The two circular loci shown in Fig. 2 represent the maximum and minimum radii of input admittance circles obtained from measurements on six devices. It can be seen that all devices measured were stable with a load conductance of 200μS and an unterminated input.

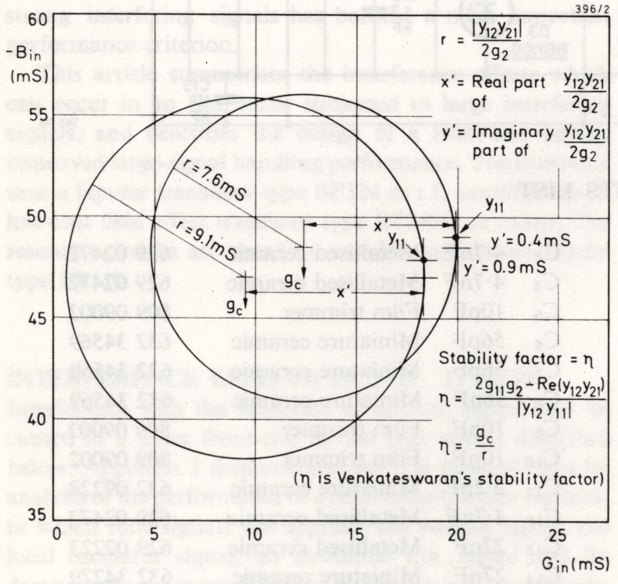

Fig. 2—Locus of input admittance of BF324: maximum and minimum radii of measured samples (load conductance = 200μS)

The optimum-noise source susceptance for the BF324 was found to range between −10pF and −15pF for the six samples measured. With the source susceptance set to approximately −12pF the effect of varying the source conductance was observed and the measured results for a typical device showing the variation of transducer gain, noise figure and cross-modulation are shown in Fig. 3a. The transducer gain shown includes a 3dB insertion loss in the collector tuned circuit, and the cross-modulation was measured using the simulated single-sideband arrangement shown in Fig. 3b, in conjunction with a spectrum analyser.

The measurements show that adequate transducer gain and very good signal handling will result if the BF324 is operated from the optimum-noise source conductance of 8·3mS. The device has excellent linearity, and so input selectivity need not be employed. This avoids the added circuit complexity and degradation of noise performance associated with a tuned aerial coupling.

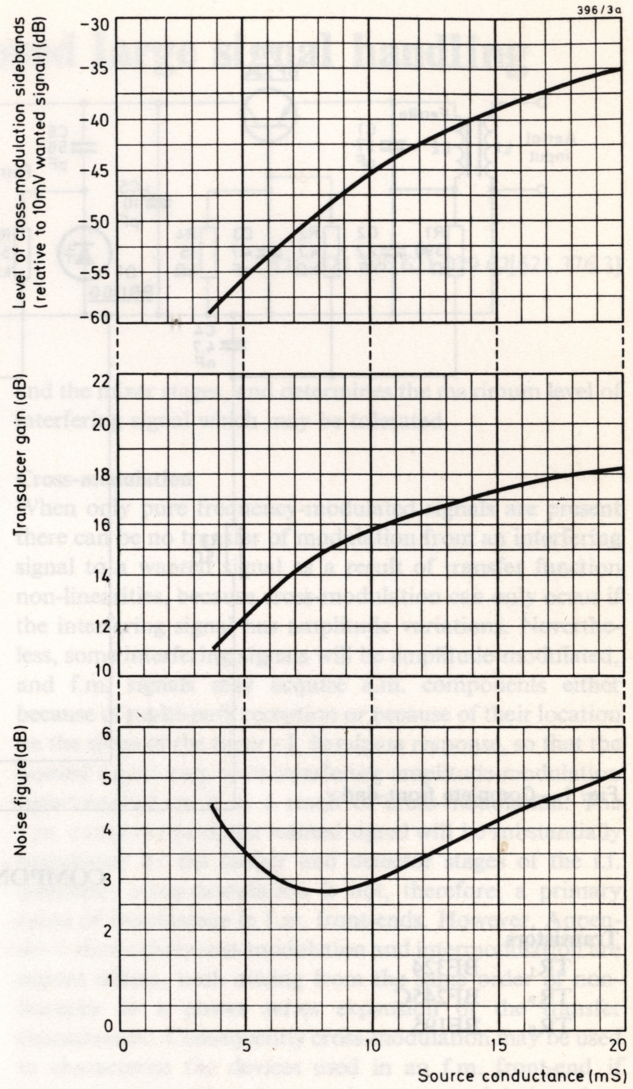

Fig. 3a—Performance of BF324 as r.f. amplifier

The r.f. stage is coupled to the mixer via a double tuned band-pass transformer employing mutual inductance 'proximity' coupling. The tuned circuit parameters at 100MHz are:—

Unloaded primary and secondary Q	$Q_{op} = Q_{os} =$	120
Loaded Q	$Q_{lp} = Q_{ls} =$	100
Coupling factor kQ		1
3dB bandwidth		1·5MHz
Attenuation at repeat spot frequency		32dB
Attenuation at image frequency		44dB
Insertion loss		10dB

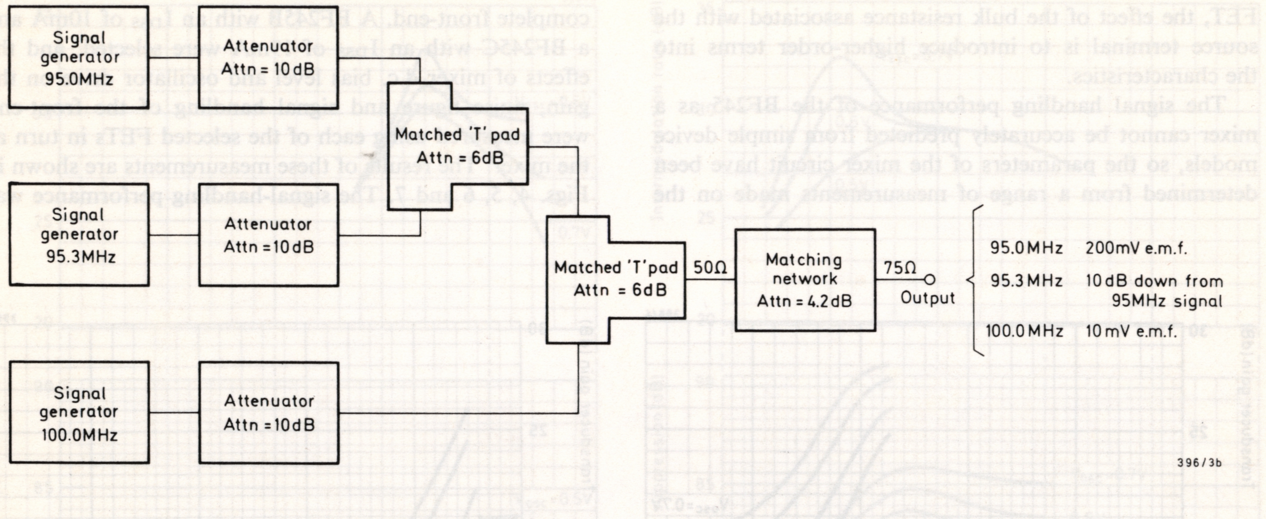

Fig. 3b—Arrangement for measuring cross-modulation

The overall transducer gain of the r.f. stage and band-pass filter is 8dB, and the r.f. stage has an adequate stability margin when operated with an uncoupled collector-tuned circuit.

Mixer stage

A junction FET type BF245 is used in the mixer stage as it affords nearly square-law mixing and useful conversion gain at low cost.

The BF245 may be operated as a mixer in three different configurations:—

1) *R.F. signal applied to the gate, oscillator signal to the source.*
This configuration gives a high overall front-end gain since the r.f. signal does not need to be tapped down to match into the high input resistance at the mixer gate (≃ 10kΩ). A high power oscillator is necessary to deliver the required 0·7V r.m.s. oscillator drive into the low-resistance source terminal (≃ 120Ω). The necessarily tight coupling between the oscillator and the mixer results in oscillator pulling, and to ensure that this does not occur for aerial signals of less than 100mV e.m.f. the r.f. signal at the mixer gate must be reduced by tapping down, thus reducing the front-end gain.

2) *R.F. signal applied to the source, oscillator signal to the gate.*
This configuration gives complete freedom from oscillator pulling as the oscillator circuit is isolated from the r.f. signal. In addition the low oscillator power requirements allow optimum design of the oscillator for low noise and good stability. The resulting front-end gain is about 10dB lower than that obtained with configuration 1, as the r.f. signal must be tapped down to match into the low-resistance source, and the transconductance in common-gate is lower than for the common-source connection.

3) *R.F. and oscillator signals applied to the gate.*
This is the configuration adopted for the front-end design. It combines some of the advantages of both the above configurations: the higher gain of configuration 1 can be realised with the low oscillator power requirements of configuration 2. The oscillator is applied to the gate in series with the r.f. signal and the consequent loose coupling between r.f. and oscillator circuits gives freedom from oscillator pulling for aerial input signal levels up to 250mV e.m.f. (75Ω).

Initial design of the mixer circuit was based on the assumption that a junction FET has a substantially square law characteristic over the range $0 < V_{GS} < V_p$ (these terms are defined in Appendix 3). The conversion gain, given by $\frac{g_{mo}|E_o|}{2V_p}$, is directly dependent on the level of oscillator injection, but for square-law operation the peak-to-peak level of oscillator plus r.f. signal must not exceed the pinch-off voltage. For an aerial input of 100mV e.m.f. the r.f. signal level at the mixer will exceed 1V r.m.s. and so, for a pinch-off voltage of 5V, the oscillator injection level must not exceed 0·7V r.m.s. and the conversion gain will be $(g_{mo}/10)$. To ensure a suitably high pinch-off voltage the BF245C (high I_{DSS} selection) was chosen. The output circuit of the FET can only be assumed to be linear provided that the output voltage swing does not exceed $V_{supply} - V_p$. This condition obviously determines the maximum i.f. load which can be used in the drain circuit.

In practice the junction FET does not have an ideal square-law input characteristic and, as is shown in Appendix 3, even if the ideal square-law characteristic is obtained by using a MOS FET or a delta-junction

FET, the effect of the bulk resistance associated with the source terminal is to introduce higher-order terms into the characteristics.

The signal handling performance of the BF245 as a mixer cannot be accurately predicted from simple device models, so the parameters of the mixer circuit have been determined from a range of measurements made on the complete front-end. A BF245B with an I_{DSS} of 10mA and a BF245C with an I_{DSS} of 19mA were selected, and the effects of mixer d.c. bias level and oscillator drive on the gain, noise figure and signal handling of the front-end were measured using each of the selected FETs in turn as the mixer. The results of these measurements are shown in Figs. 4, 5, 6 and 7. The signal-handling performance was assessed by measurement of the repeat spot suppression relative to a wanted carrier level of 20μV e.m.f., and by measuring the relative level of interfering signal (spaced 400kHz from a 1mV e.m.f. wanted signal) which gave rise to 1% intermodulation.

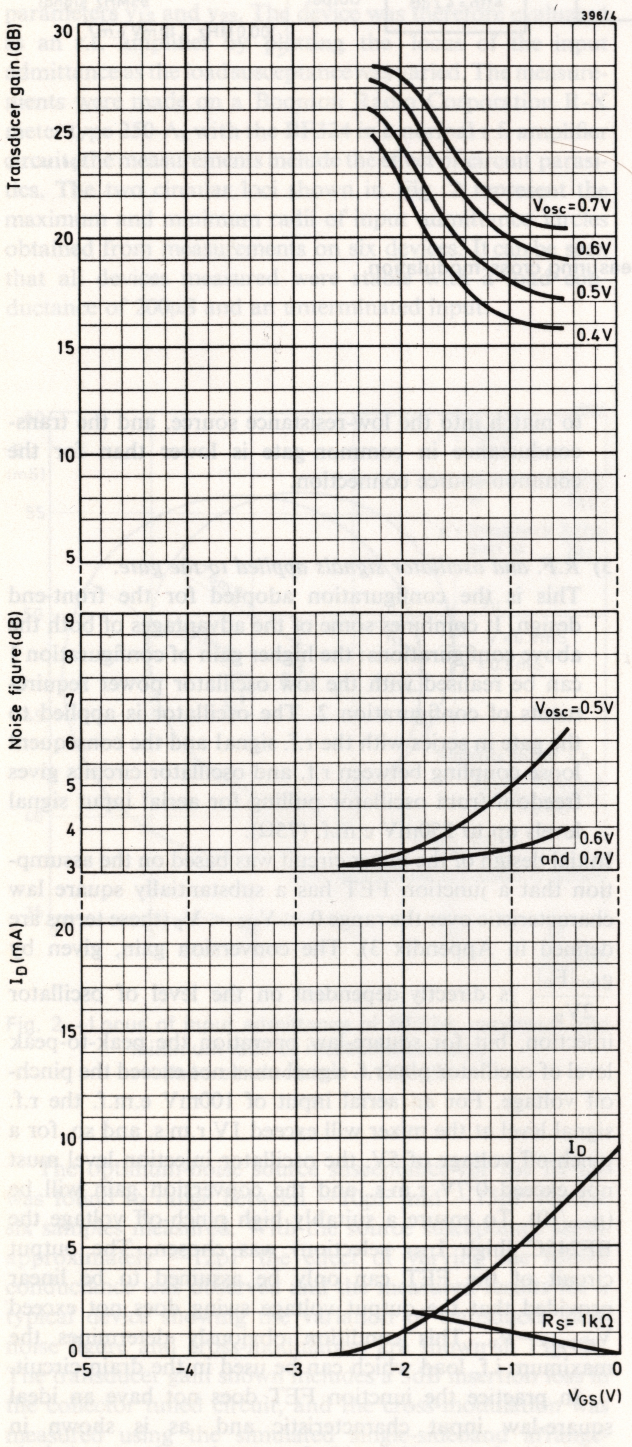

Fig. 4—Input characteristic of BF245B (I_{DSS} = 10mA). Front-end gain and noise figure as functions of V_{GS} and V_{osc}

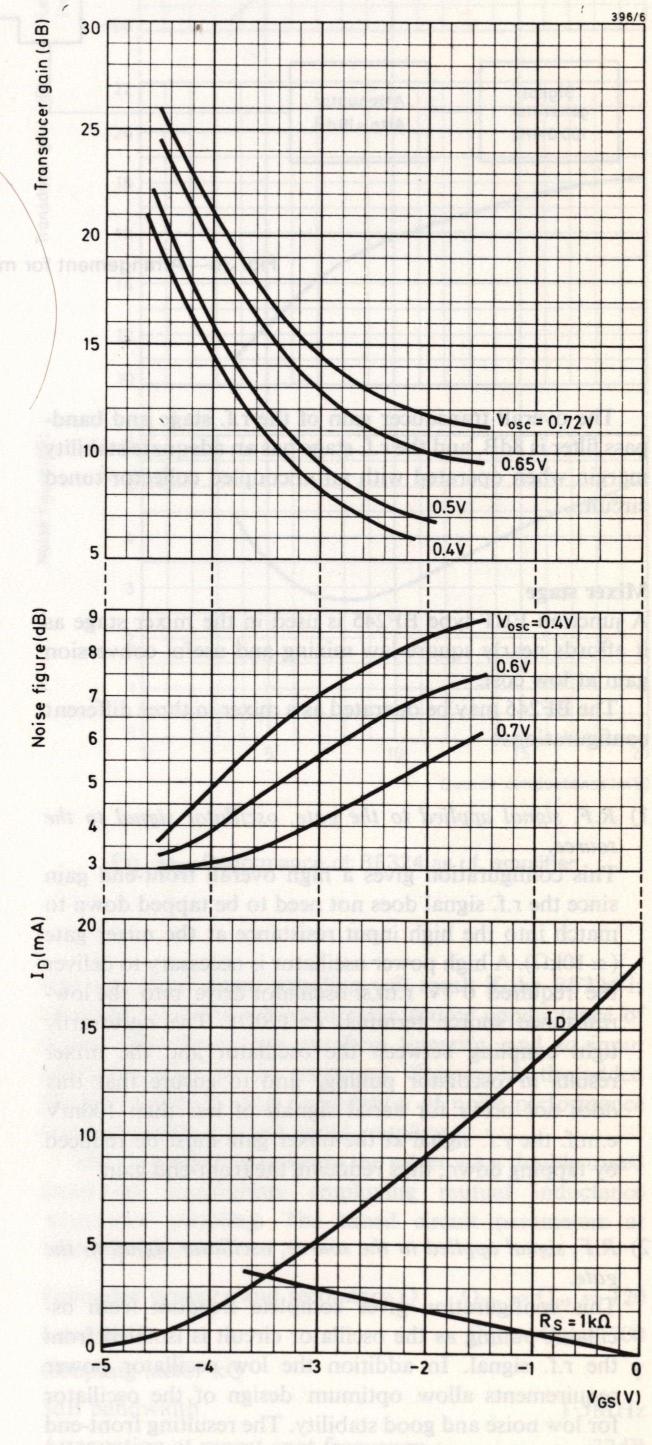

Fig. 5—Input characteristic of BF245C (I_{DSS} = 19mA). Front-end gain and noise figure as functions of V_{GS} and V_{osc}

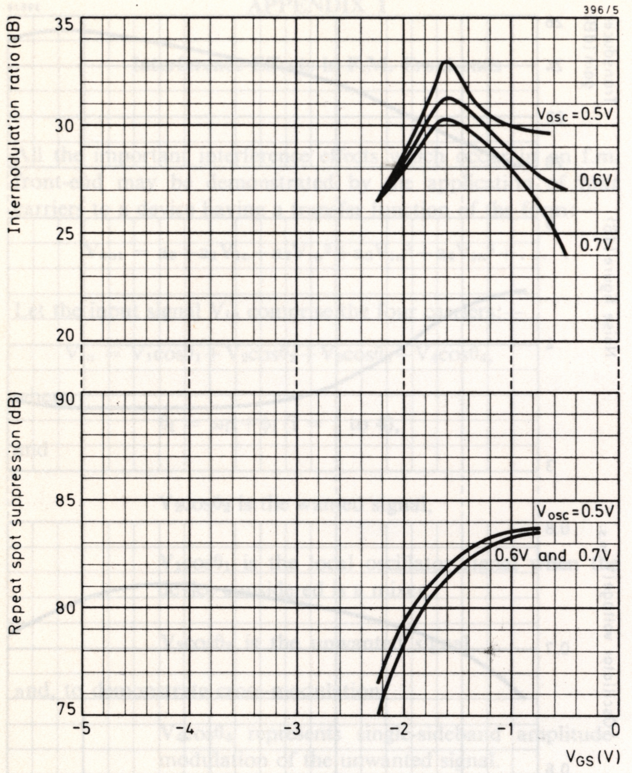

Fig. 6—Front-end signal-handling performance with BF245B

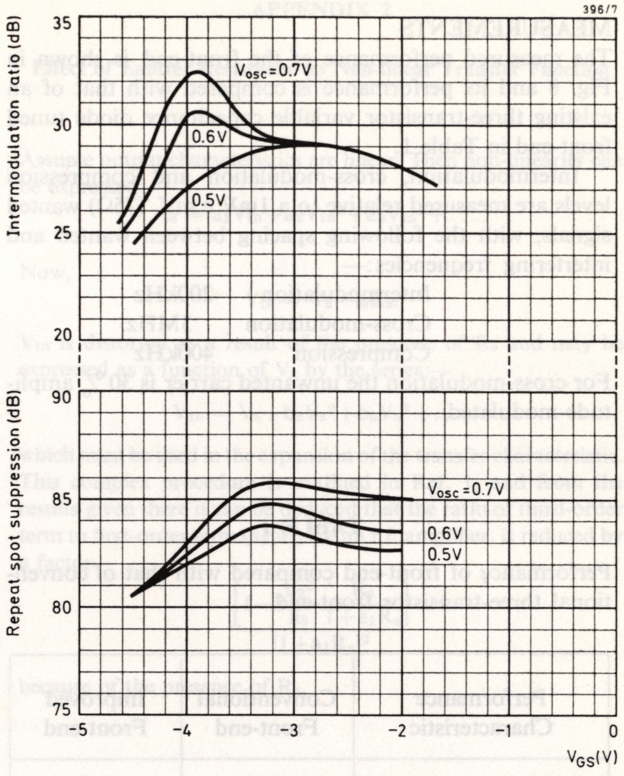

Fig. 7—Front-end signal-handling performance with BF245C

From these results, and the measured input characteristics also shown in Figs. 4 and 5, it can be seen that the selection of a 1kΩ resistor in the source as an auto-bias resistor and an oscillator injection level of 0·7V r.m.s. ensures adequate front-end performance for the full spread of mixer devices. The measurements were made with a single tuned circuit presenting an i.f. load of 10kΩ in the mixer drain; the insertion loss was 3dB and the i.f. bandwidth was 300kHz. Under the chosen operating conditions the mixer is contributing about 1dB to the front-end noise figure. This contribution could be reduced only at the expense of mixer signal handling, by increasing the r.f. gain.

The oscillator circuit

The oscillator uses a BF195 transistor in a conventional common-base circuit. The transistor is operated at I_c = 1mA and V_{ce} = 9V, to ensure low noise and good stability. The level of oscillator signal injection is adjusted by varying the proximity coupling between the oscillator tank circuit and the series injection loop.

Tuned circuits

The primary and secondary of the r.f. band-pass tuned circuit, and the oscillator tank circuit, are tuned by variable capacitance diodes type BB110G.

The minimum permissible value of tuning voltage is determined by the requirement for a constant oscillator injection level; at the low-frequency end of the band the tuning voltage must be large enough to prevent the oscillator swing across the tank circuit being restricted by forward biasing of the diode. The maximum tuning voltage which may be used is determined by the maximum continuous voltage of the diode.

In the present design the tuning voltage swing employed is the maximum permitted by these conditions, that is, from 3 to 30V. The aerial frequency range required is 87·5 to 108MHz, and sufficient capacitance swing for this is achieved by using a 56pF capacitor in series with the variable capacitance diode. This series capacitor has the lowest possible value to reduce the r.f. swing across the diode, and hence minimise the effects of diode non-linearity.

The maximum tuning voltage may be reduced to about 20V and the series capacitor increased to 100pF without serious degradation of tuner performance, but for a maximum tuning voltage of less than 20V a back-to-back variable capacitance diode should be used, as it has superior signal-handling ability.

MEASUREMENTS

The measured performance of the front-end is shown in Fig. 8 and its performance is compared with that of an existing three-transistor variable capacitance diode tuned front-end in Table 1.

Intermodulation, cross-modulation and compression levels are measured relative to a 1mV e.m.f. (75Ω) wanted signals, with the following spacing between wanted and interfering frequencies:—

Intermodulation	200kHz
Cross-modulation	3MHz
Compression	400kHz

For cross-modulation the unwanted carrier is 30% amplitude-modulated.

TABLE 1

Performance of front-end compared with that of conventional three-transistor front-end.

Performance Characteristic	Conventional Front-end	Improved Front-end
Transducer gain	26dB*	22dB
Noise figure	8dB	4dB
Repeat spot suppression relative to a 20μV e.m.f. wanted signal	54dB	82dB
Level of interfering signal for 1% intermodulation	14dB	26dB
Level of interfering signal for 1% cross-modulation	19dB	30dB
Level of interfering signal for 3dB compression	28dB	38dB
Signal level for 5kHz oscillator pulling	25mV e.m.f.	>250mV e.m.f.

*Three-transistor front-end has double-tuned i.f. transformer, a tuned aerial input and a single tuned circuit coupling r.f. and mixer stages.

REFERENCE

1. 'Cross-modulation and modulation distortion in a.m. receivers equipped with transistors'. **Electronic Applications**, Vol. 20, 1959-1960, No. 3, pp 107 to 127.

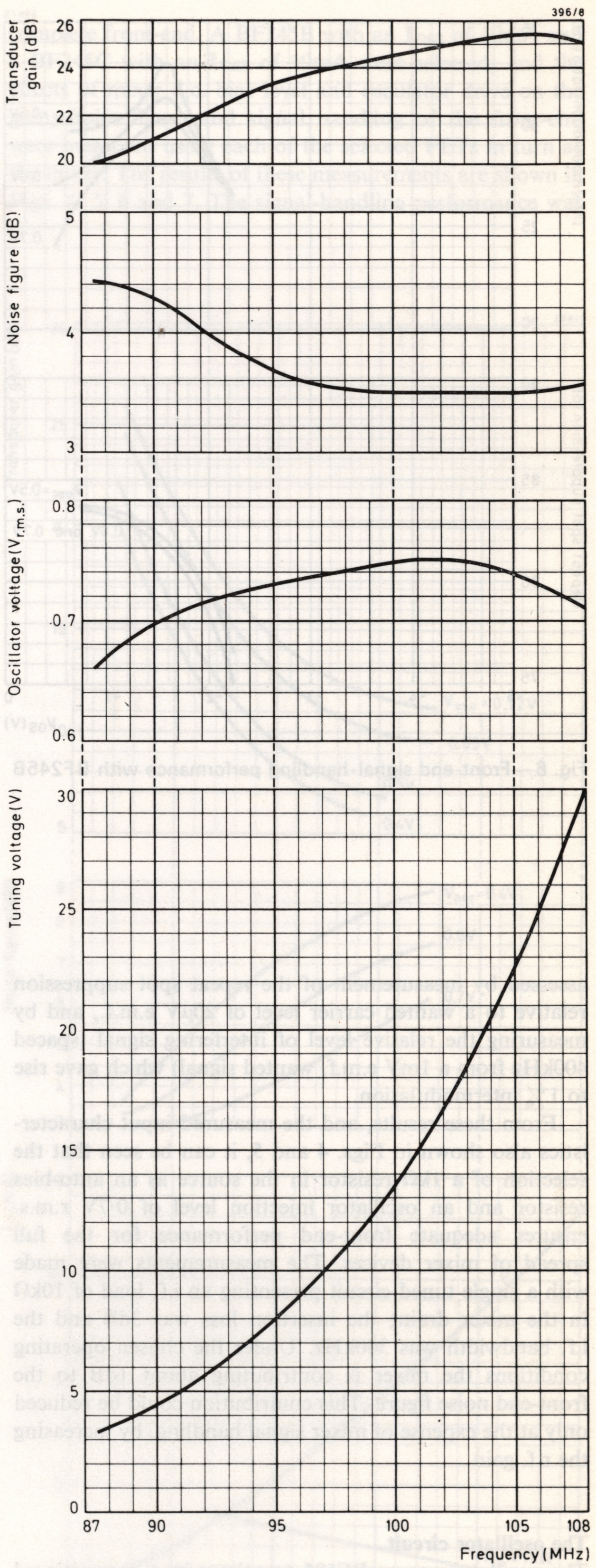

Fig. 8—Typical measured performance of complete front-end

APPENDIX 1

Interference Effects in F.M. Front-ends

All the important interference effects which occur in an f.m. front-end may be demonstrated by the application of four carriers to a device having a transfer function of the form:—

$$V_{out} = a_0 + a_1V_{in} + a_2V_{in}^2 + a_3V_{in}^3 + a_4V_{in}^4 + \ldots .$$

Let the input signal V_{in} comprise the four carriers:—

$$V_{in} = V_1\cos\theta_1 + V_2\cos\theta_2 + V_3\cos\theta_3 + V_4\cos\theta_4,$$

where

$$\theta_i = \omega_it + \phi_i \ (i = 1 \text{ to } 4),$$

and

$V_2\cos\theta_2$ is the wanted signal,

$V_1\cos\theta_1$ is the local oscillator signal when the device considered is a mixer,

$V_3\cos\theta_3$ is the unwanted signal,

and, to demonstrate cross-modulation,

$V_4\cos\theta_4$ represents single-sideband amplitude-modulation of the unwanted signal.

The relevant terms in the expansion of V_{out} are:—

(Term)

$$V_{out} = a_1V_2\cos\theta_2 + \ldots a_1V_3\cos\theta_3 + \ldots \quad (1)$$

$$+ a_2V_1V_2\cos(\theta_1 - \theta_2) + \ldots a_2V_1V_3\cos(\theta_3 - \theta_1) + \ldots \quad (2)$$

$$+ (3/4)a_4V_1^2V_3^2\cos2(\theta_1 - \theta_3) + \ldots \quad (3)$$

$$+ (3/4)a_3V_2^2V_3\cos(2\theta_2 - \theta_3) + \ldots \quad (4)$$

$$+ (3/2)a_4V_1V_2^2V_3\cos[\theta_1 - (2\theta_2 - \theta_3)] + \ldots \quad (5)$$

$$+ (3/2)a_3V_2V_3V_4[\cos(\theta_2 + \theta_3 - \theta_4) + \cos(\theta_2 - \theta_3 + \theta_4)] + \ldots \quad (6)$$

$$+ 3a_4V_1V_2V_3V_4[\cos\{\theta_1 - (\theta_2 + \theta_3 - \theta_4)\} + \cos\{\theta_1 - (\theta_2 - \theta_3 + \theta_4)\}] + \ldots \quad (7)$$

(Term)

(1) Linear amplification gives wanted output from r.f. stage and i.f. response in the mixer.

(2) Conversion of wanted signal to i.f. in mixer. Image response when $\theta_3 = \theta_2 + 2(\text{i.f.})$.

(3) Repeat spot interference when $\theta_3 = \theta_1 - \frac{\text{i.f.}}{2}$.

(4) Intermodulation in the r.f. amplifier. Here θ_2 and θ_3 represent unwanted carriers; the wanted carrier is at $2\theta_2 - \theta_3$.

(5) Intermodulation in the mixer, where θ_2 and θ_3 are as above.

(6) Cross-modulation in the r.f. amplifier. As θ_4 represents modulation sideband, $\theta_4 = \theta_3 + \theta_m$ so that term $\theta_2 \pm \theta_m$ results.

(7) Cross-modulation in the mixer. Terms $\theta_1 - (\theta_2 \pm \theta_m)$ are produced.

APPENDIX 2

Effect of Emitter Resistance on Non-linear Transfer Function

Assume output characteristics are linear. Then non-linearity can be expressed:—

$$i_e = a_1V_{in} + a_2V_{in}^2 + a_3V_{in}^3 + \ldots,$$

Now,

$$V_{in} = V_s - i_eR_s.$$

V_{in} is distorted as a result of the presence of R_s and may be expressed as a function of V_s by the series:—

$$V_{in} = V_s + b_2V_s^2 + b_3V_s^3 + \ldots,$$

which must be used in the expansion of the transfer characteristic. This complex procedure is outlined in Ref. 1, and from the results given there it can be deduced that the ratio of third-order term to first-order term (a_3/a_1) for an r.f. amplifier, is reduced by a factor

$$\frac{\left[1 - 2\frac{a_2^2}{a_3} \cdot \frac{R_s}{1 + a_1R_s}\right]}{[1 + a_1R_s]^3}$$

because of the presence of R_s.

APPENDIX 3

FET Characteristics

The performance of a FET as the mixer stage in an f.m. front-end can be analysed as follows. Let

V_p = pinch-off voltage
I_{DSS} = drain current at $V_{GS} = 0$
$g_{mo} = g_m$ at $V_{GS} = 0$

For an ideal square-law device:—

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$

where

V_{GS} = gate bias

and

$$I_{DSS} = \frac{g_{mo}V_p}{2}.$$

When a local oscillator signal $E_o\cos\omega_ot$ and an r.f. signal $E_s\cos\omega_st$ are applied between gate and source terminals, the i.f. drain current

$$i_{D(\text{i.f.})} = \frac{g_{mo}E_oE_s}{2V_p}\cos(\omega_s - \omega_o)t,$$

and the conversion conductance

$$g_c = \left|\frac{i_{D(\text{i.f.})}}{E_s}\right| = \frac{g_{mo}\,|E_o|}{2V_p},$$

where

$|E_o|$ = peak value of oscillator drive.

Effect of bulk resistance in source terminal

The voltage drop across the bulk source resistance R_S contributes to the effective input voltage, V_{GS}, as follows:

$$V_{GS} = V_{in} + i_D R_S$$

and

$$i_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$

then

$$V_{in} = V_p\left[1 - \frac{i_D R_S}{V_p} - \sqrt{\frac{i_D}{I_{DSS}}}\right]$$

The characteristic may be expressed as a Taylor series about the operating point I_D:

$$i_D = I_D + \alpha_1 V_{in} + \frac{\alpha_2}{2} V_{in}^2 + \frac{\alpha_3}{6} V_{in}^3 + \ldots$$

The coefficients α_1, α_2, α_3 etc. may be found by successive differentiation:

$$\alpha_1 = 2\frac{\sqrt{I_{DSS}\ I_D}}{V_p D}$$

$$\alpha_2 = \frac{2I_{DSS}}{V_p^2 D^3}$$

$$\alpha_3 = \frac{12R_S . I_{DSS}^2}{V_p^4 D^5}$$

$$\alpha_4 = \frac{120R_S^2 . I_{DSS}^3}{V_p^6 D^7}$$

where

$$D = \frac{1}{V_p}\left(V_p + 2R_S\sqrt{I_{DSS} . I_D}\right).$$

The third- and fourth-order coefficients are produced as a result of the presence of R_S.

This analysis is only valid at low frequencies since gate-drain and gate-source capacitances must be considered at higher frequencies, and it can be shown that the junction FET has a transfer function of the form

$$I_D = I_{DSS}\left[1 - \frac{3V_{GS}}{V_p} + 2\left(\frac{V_{GS}}{V_p}\right)^{1\cdot5}\right]$$

rather than the ideal square-law assumed.

A survey of converter circuits for switched-mode power supplies

L. E. Jansson
Mullard Central Application Laboratory

UDC 621.314.12:621.311.68.[621.376.54]

Seven types of d.c.-to-d.c. converter are described. These are: single-transistor flyback (ringing-choke), two-transistor flyback, single-transistor forward, two-transistor forward, single-ended push-pull, push-pull, and bridge. Choice of circuit for various applications is discussed. Push-pull circuits are recommended for high-performance, low-voltage power supplies; forward converters are suitable for similar supplies at lower powers; and flyback converters are suitable for use in high-voltage supplies and in multi-output instrument supplies.

INTRODUCTION

The basic arrangement of a switched-mode power supply is shown in Fig. 1. In this system, the mains input is first rectified and smoothed and the resulting d.c. voltage is chopped at high frequency (> 20kHz) by a switch. The chopped waveform is applied to the primary of a transformer and the signal at the secondary is rectified and filtered to give the required d.c. output. This is sensed by the control circuit and a correction signal is produced which is used to vary the mark/space ratio of the switched waveform and thus compensate for any change at the output. The same system can operate, without the rectifier, from a battery or any other d.c. input.

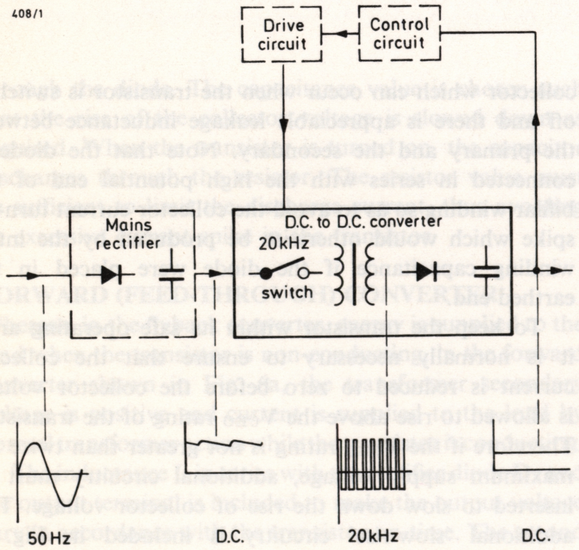

Fig. 1—Schematic diagram of switched-mode power supply

A variety of circuits are available to convert the d.c. input voltage to the required d.c. output voltage. In this article, seven such circuits, all of which provide isolation between the input and the output, are examined. The circuits range from the single-transistor flyback (ringing-choke) converter and the single-transistor forward (feed-through) converter, to the four-transistor full-bridge circuit, from which other 'half-bridge' circuits can be derived. For comparison an eighth circuit, the simple series regulator, is also briefly described.

To facilitate explanation of the range of circuits considered, brief descriptions are first given of the two basic circuits, the flyback converter and the forward converter, after which the choice of circuit appropriate to various power supply requirements is discussed.

FLYBACK (RINGING-CHOKE) CONVERTER

The circuit of a flyback converter, and its associated waveforms, are shown in Figs. 2a, b, and c. When the switch is closed, the supply voltage is connected across the inductance and the output diode is non-conducting. Current rises linearly in the inductance until the switch is opened; at this point, the voltage across the inductance reverses and the energy stored is transferred into the output reservoir capacitor and the load.

The voltage and current waveforms shown in Fig. 2b apply when the on- and off-times of the switch are equal, giving an output voltage equal and opposite to the input voltage (ignoring the voltage drop across the diode). The waveforms of Fig. 2c show the effects of halving the on-time of the switch and keeping the operating frequency

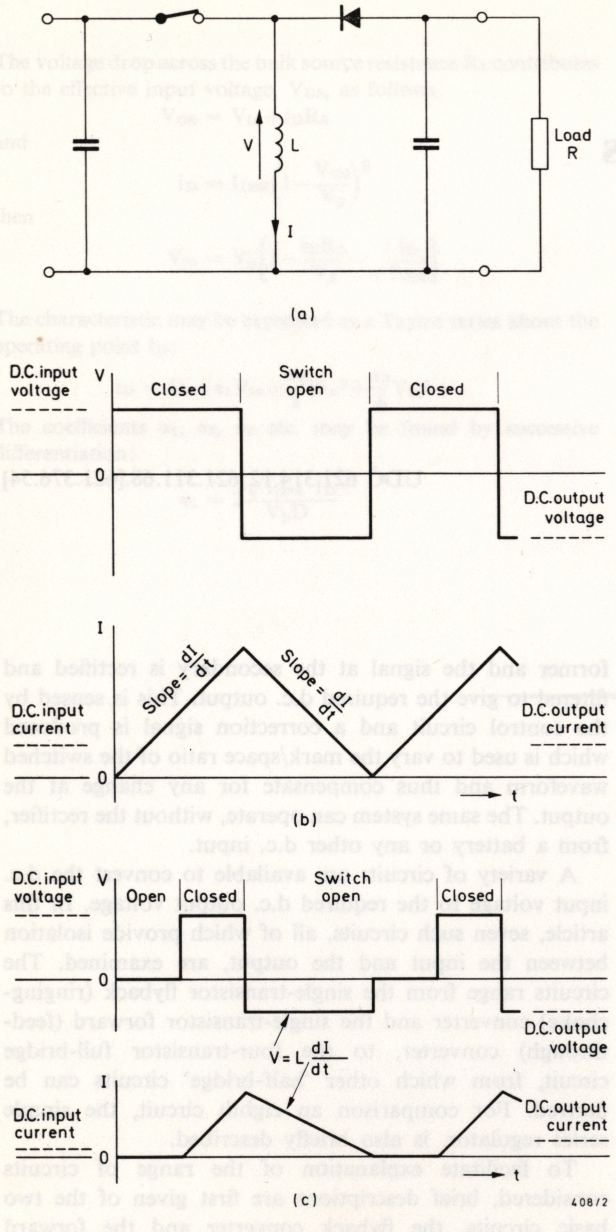
V
L
I
Load R
(a)
D.C.input voltage
V
Closed
Switch open
Closed
0
D.C.output voltage
I
Slope = dI/dt
Slope = −dI/dt
D.C.input current
D.C.output current
0
t
(b)
D.C.input voltage
Open
Closed
Switch open
Closed
0
D.C.output voltage
V = L dI/dt
D.C.input current
D.C.output current
0
(c)
408/2

Fig. 2—(a) Basic flyback converter
(b) Waveforms for equal on- and off-times
(c) Waveforms with on-time halved

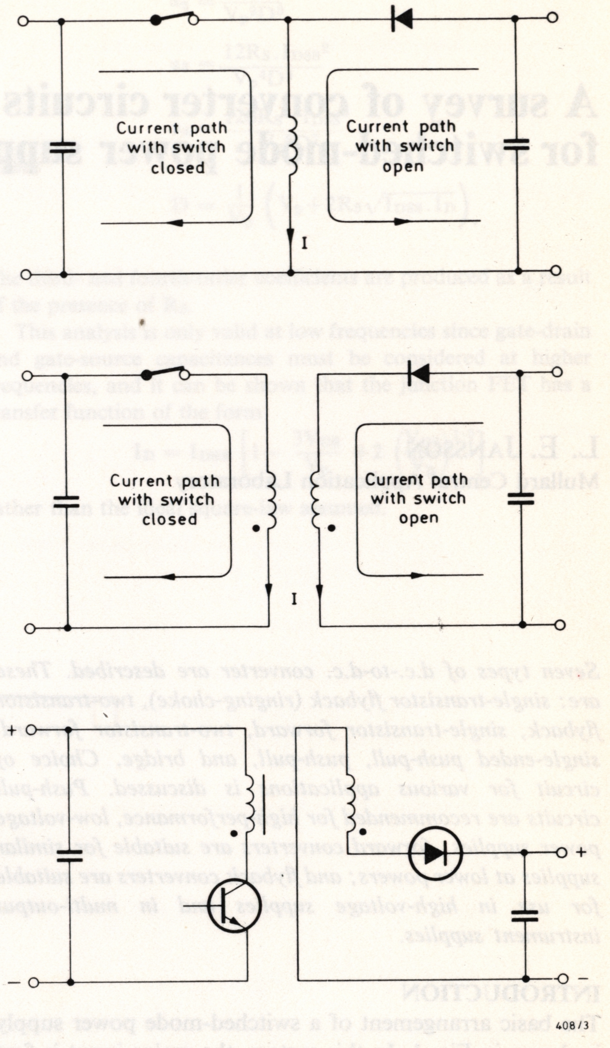
Current path with switch closed
Current path with switch open
I
Current path with switch closed
Current path with switch open
I
+
−
408/3

Fig. 3—Development of practical flyback converter circuit

and load resistance constant. This results in the output voltage being halved, and demonstrates one method of controlling the output of a switched-mode power supply.

In Fig. 3, the basic circuit of Fig. 2 is developed into a practical circuit which uses a double wound inductor and a transistor switch. To limit the maximum voltage across the transistor to twice the supply voltage, an additional winding and diode can be employed, as shown in Fig. 4. This winding returns the energy stored in the inductance to the supply if the circuit is operated with no load on the secondary. The additional winding is bifilar wound with the primary to ensure low leakage inductance between these windings. The extra winding also limits the amplitude of the voltage spike at the transistor collector which can occur when the transistor is switched off and there is appreciable leakage inductance between the primary and the secondary. Note that the diode is connected in series with the high potential end of the bifilar winding so as to avoid the collector current turn-on spike which would otherwise be produced by the inter-winding capacitance if the diode were placed in the earthed end.

To keep the transistor within its safe operating area, it is normally necessary to ensure that the collector current is reduced to zero before the collector voltage is allowed to rise above the V_{CEO} rating of the transistor. Therefore if the V_{CEO} rating is not greater than twice the maximum supply voltage, additional circuitry must be inserted to slow down the rise of collector voltage. This additional 'slow-rise' circuitry is included in Fig. 5. When the transistor is switched off, the transformer current is diverted into the capacitor which charges through the diode. The capacitance value is chosen such that the rise of the collector voltage is slowed down as required. When the transistor is turned on, the capacitor discharges through the resistor. The resistor value must be sufficient to limit the discharge current, thus avoiding an excessive current spike in the transistor.

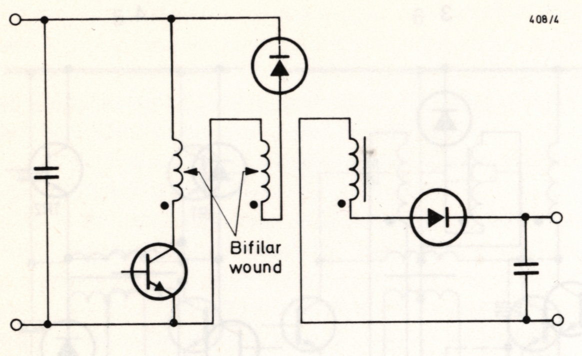
408/4
Bifilar wound

Fig. 4—Flyback converter with voltage limiting circuit

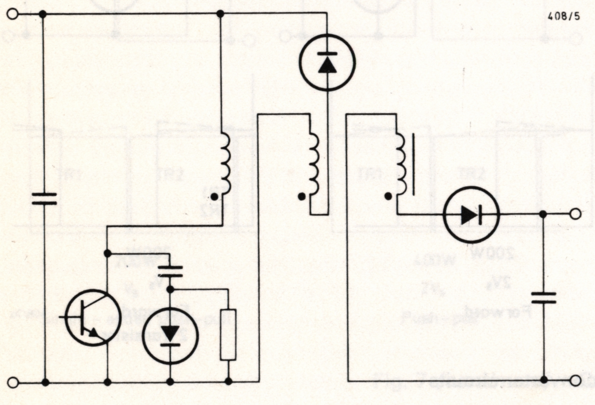

Fig. 5—Flyback converter with added 'slow-rise' circuit

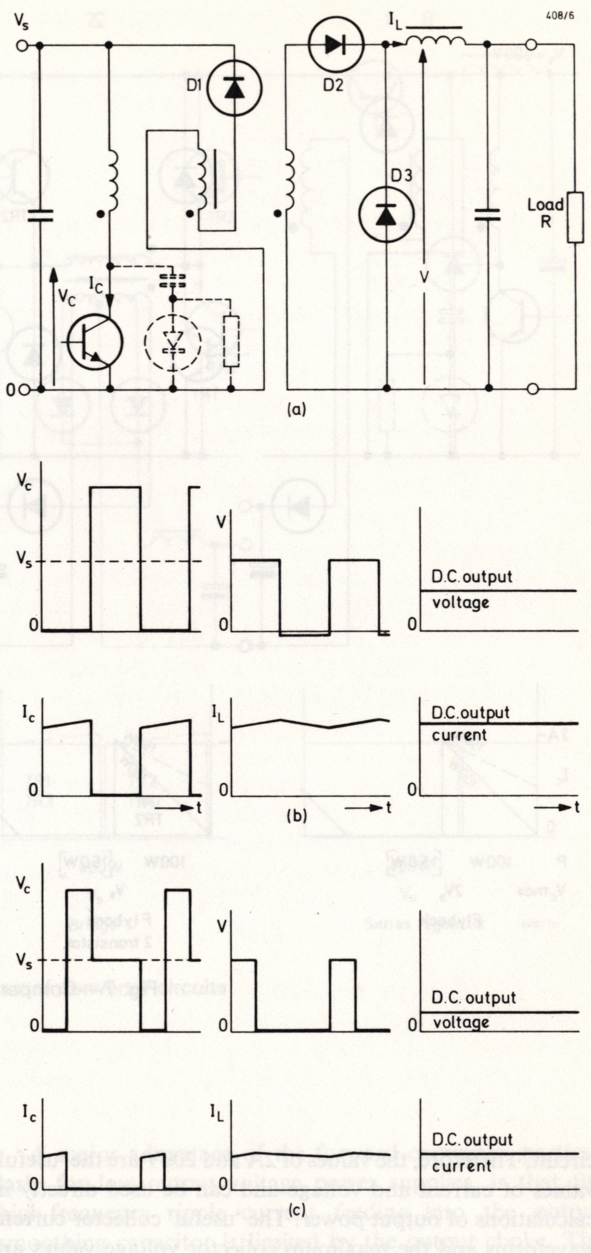
V_s
I_L
408/6
D1
D2
D3
Load R
V
V_c
I_c
0
(a)
V_c
V_s
0
V
0
D.C.output voltage
0
I_c
0
t
I_L
0
t
D.C.output current
0
t
(b)
V_c
V_s
0
V
0
D.C. output voltage
0
I_c
0
I_L
0
D.C. output current
0
(c)

Fig. 6—(a) Forward converter
(b) Waveforms for equal on- and off-times
(c) Waveforms with on-time halved

FORWARD (FEED-THROUGH) CONVERTER

Whereas, in the flyback converter, energy is supplied to the load when the transistor is non-conducting, in the forward converter shown in Fig. 6a, the transformer secondary voltage is positive and current is supplied to the load by normal transformer action while the transistor is conducting.

The inductance L in series with the rectifier diode D_2 and the output terminal is included to make the output voltage vary in accordance with the transistor on-time. The second diode D_3 provides a path for the output current which continues to be supplied by L when the transistor is not conducting. When the transistor is off, the transformer magnetizing current is returned to the supply via the additional winding, bifilar wound with the primary, and the diode D_1.

Examples of voltage and current waveforms are shown in Figs. 6b, and c.

SURVEY OF CONVERTER CIRCUITS

In Fig. 7, eight circuits are compared and the output power obtainable from each circuit is indicated for an example where the peak current in all transistors is assumed to be 2A, and the supply voltage, 200V. Circuit losses are ignored to simplify the description of the main properties of each

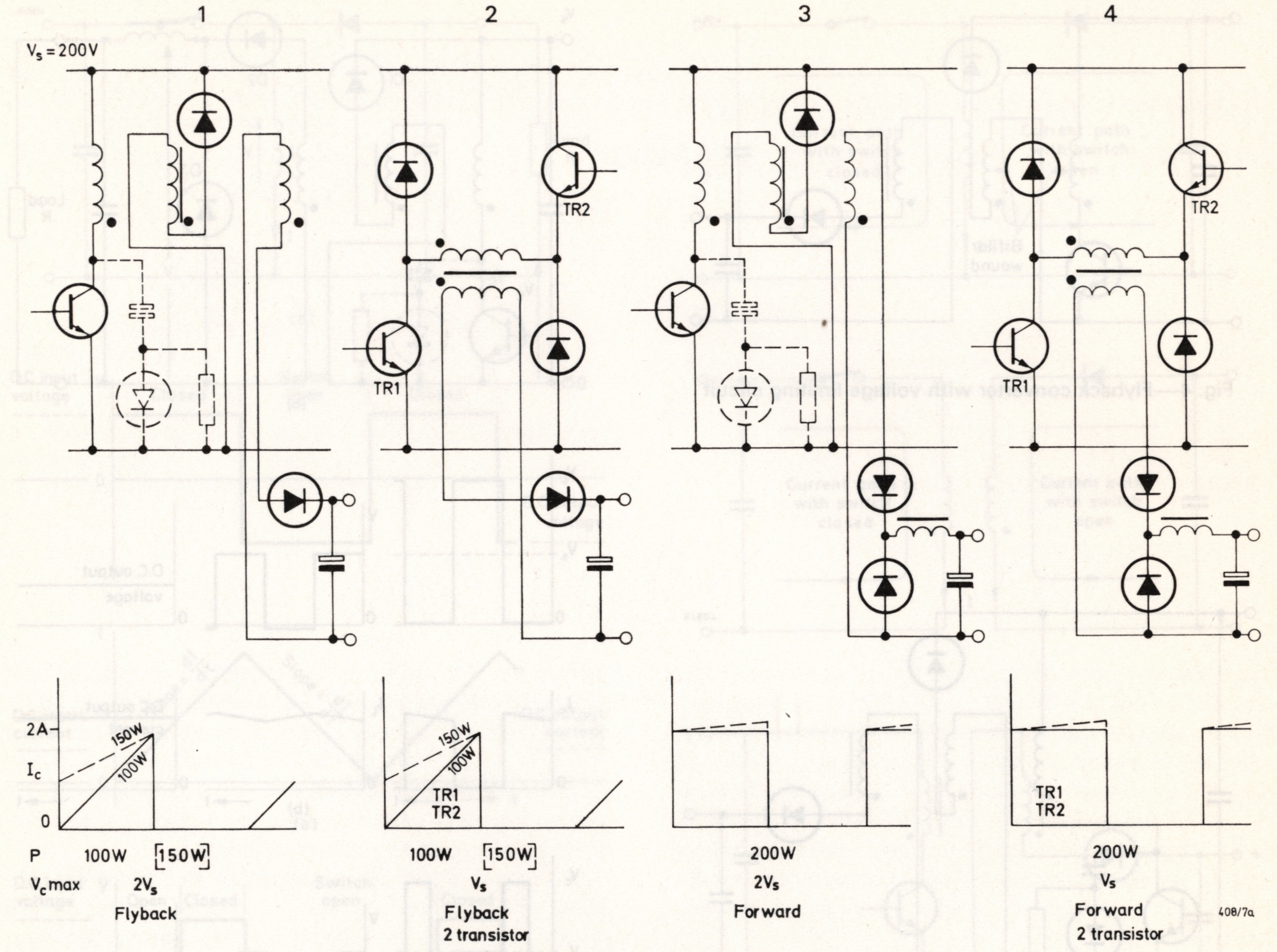

Fig. 7—Comparison of converter circuits

circuit. Therefore, the values of 2A and 200V are the 'useful' values of current and voltage and can be used directly in calculations of output power. The 'useful' collector current waveforms and the maximum collector voltage values are given for each circuit. Factors affecting practical collector current and voltage levels, together with choice of transistor, are considered later on page 6.

Circuit 1

Circuit 1 is the basic flyback converter circuit already described. The optional slow-rise circuit, also described earlier, is drawn in broken line. The collector current waveform (solid line) has an average value of 0·5A over a full cycle so that the input and output powers (ignoring losses) are 100W, or one quarter of the product $V_S I_{C(pk)}$ for a 50% on-time.

The output power can be raised, without increasing the peak collector current, by switching the transistor on before the transformer current has fallen to zero. It is then necessary to use a more expensive transformer. In the example shown by the dotted current waveform, the inductance is doubled and the transistor is switched on when the transformer current is 1A so as to achieve a peak current of 2A as before. The average input current now becomes 0·75A, and the output power is increased to 150W.

Circuit 2

In this two-transistor version of the flyback converter, which can be regarded as a diagonal half-bridge circuit, both transistors are switched on simultaneously and, while the transistors conduct, the current waveform in the transformer primary is identical to that in Circuit 1. Similarly, the voltage across the transformer primary is identical to that in Circuit 1. However, whereas in Circuit 1 the collector voltage of the transistor can rise to twice the supply voltage, in Circuit 2 both ends of the transformer primary change their potential by an amount equal to the supply voltage. Therefore, the voltage across the transformer windings remains as in Circuit 1, but the maximum collector voltage on the transistors does not exceed the supply voltage. The reverse voltage across the primary when the transistors are switched off is limited to that of the supply by the clamping action of the two diodes. Because the maximum collector voltage is limited to that of the supply, the slow rise circuit (shown with broken line in circuit 1) can be omitted provided that the transistor V_{CEO} rating is not less than the maximum supply voltage.

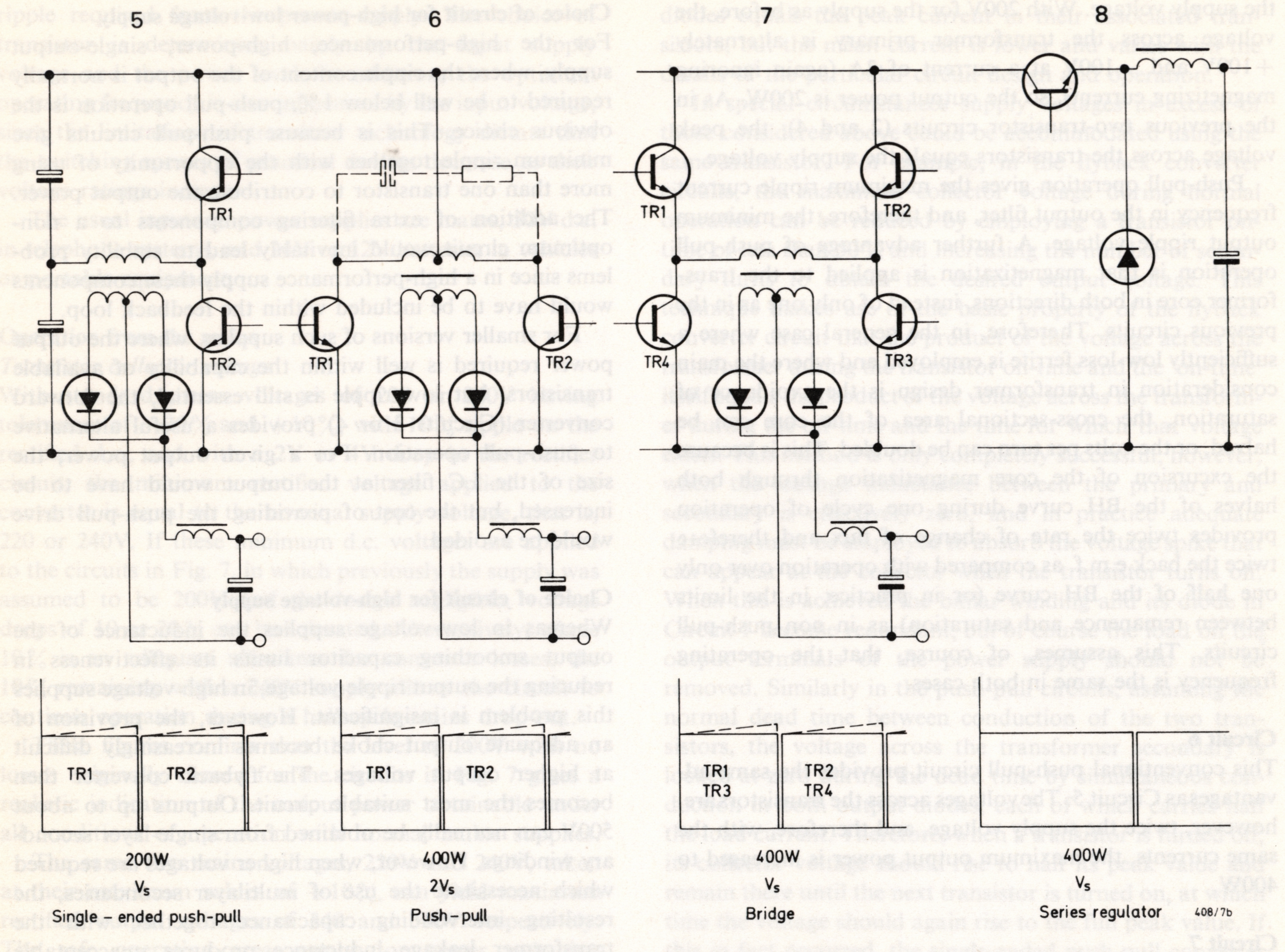

Fig. 7 *(continued)*—Comparison of converter circuits

Circuit 3

Circuit 3 is the forward converter described earlier (page 3). It can give up to twice the output power of the simple flyback converters (Circuits 1 and 2). If the output choke and transformer inductances are high, so that the time-dependent magnetizing currents, illustrated by the broken line addition to the Circuit 3 current waveform, form a negligible part of the collector current, the previously assumed collector current of 2A supplies the steady-state load current for 50% of the cycle time. This gives an average input current of 1A at 200V, or 200W power (one half of the product $V_S I_{C(pk)}$).

In practice the magnetizing currents might be 20% of the stipulated peak current, and so the maximum output of the forward converter would be comparable with that of a high-output version of the flyback circuit. Only the simplest square and sawtooth waveforms give the maximum difference in output of two times.

A major advantage of the forward converter, particularly for low output voltage power supplies, is that the high-frequency ripple current feeding into the output smoothing capacitor is limited by the output choke. The ripple voltage at the output terminals of a forward converter is therefore much less than that for a flyback converter, in which the minimum achievable ripple voltage is determined by the inductance and resistance of practical electrolytic output smoothing capacitors.

Circuit 4

Circuit 4 is the two-transistor version of the forward converter and provides the same output as the single transistor version but with half the peak voltage across the transistors. It relates to Circuit 3 as Circuit 2 relates to Circuit 1.

Circuit 5

This single-ended push-pull circuit can be regarded as the vertical half of a bridge circuit. Here the two transistors are driven alternately and, with equal conduction times, the d.c. voltage at the junction of the two capacitors equals half the supply voltage. With 200V for the supply as before, the voltage across the transformer primary is alternately +100V and −100V at a current of 2A (again ignoring magnetizing current), so the output power is 200W. As in the previous two-transistor circuits (2 and 4), the peak voltage across the transistors equals the supply voltage.

Push-pull operation gives the maximum ripple current frequency in the output filter, and therefore, the minimum output ripple voltage. A further advantage of push-pull operation is that magnetization is applied to the transformer core in both directions, instead of only one as in the previous circuits. Therefore, in the general case where a sufficiently low-loss ferrite is employed and where the main consideration in transformer design is the avoidance of saturation, the cross-sectional area of the core can be halved, or the volts per turn can be doubled. This is because the excursion of the core magnetization through both halves of the BH curve during one cycle of operation provides twice the rate of change of flux and therefore twice the back e.m.f. as compared with operation over only one half of the BH curve (or in practice, in the limits between remanence and saturation) as in non push-pull circuits. This assumes, of course, that the operating frequency is the same in both cases.

Circuit 6

This conventional push-pull circuit provides the same advantages as Circuit 5. The voltages across the transistors are, however, twice the supply voltage, and therefore, with the same currents, the maximum output power is increased to 400W.

Circuit 7

This is the full-bridge circuit. It again provides 400W but the peak voltage across the transistors is limited to that of the supply, at the expense, however, of further complication of the drive circuitry.

Circuit 8

The switching series regulator, unlike all the previous circuits, provides no isolation between the input and the output. This lack of isolation makes it unsuitable for most mains operated power supplies. Where applicable, however, it can provide the greatest output power from a given transistor. This is because the duty cycle can be up to 100%, in which case the input and output voltages and currents are equal (ignoring losses). In the example shown the output is 400W, but because the circuit includes no transformer, this maximum output is reduced to the product of the transistor current and the desired output voltage. The output voltage must always be less than the input voltage.

CHOICE OF CIRCUIT

Three main application classes of power supply can be identified; the low-voltage high-power single-output supply such as the 5V supply for a large computer; the high voltage supply; and the instrument power supply which often requires a multiplicity of outputs giving a variety of different voltages and currents.

Choice of circuit for high-power low-voltage supply

For the high-performance, high-power, single-output supply, where the ripple content of the output is normally required to be well below 1%, push-pull operation is the obvious choice. This is because push-pull circuits give minimum ripple together with the opportunity of using more than one transistor to contribute the output power. The addition of extra filtering components to a non-optimum circuit would inevitably lead to stability problems since in a high-performance supply these components would have to be included within the feedback loop.

For smaller versions of such supplies, where the output power required is well within the capability of available transistors, but low ripple is still essential, the forward converter (Circuits 3 or 4) provides a useful alternative to push-pull operation. For a given output power, the size of the LC filter at the output would have to be increased, but the cost of providing the push-pull drive would be avoided.

Choice of circuit for high-voltage supply

Whereas in low-voltage supplies the inductance of the output smoothing capacitor limits its effectiveness in reducing the output ripple voltage, in high voltage supplies this problem is insignificant. However, the provision of an adequate output choke becomes increasingly difficult at higher output voltages. The flyback converter then becomes the most suitable circuit. Outputs up to about 500V can normally be obtained from single-layer secondary windings. However, when higher voltages are required which necessitate the use of multilayer secondaries, the resulting interwinding capacitance together with the transformer leakage inductance produces unacceptable 'ringing' on the transistor current waveform. This problem can be completely overcome by providing the desired number of single-layer secondaries, each feeding its own rectifier and output capacitor, and joining the output capacitors in series to produce the required final output voltage. In this arrangement, adjacent ends of all the windings are joined by an output smoothing capacitor. In addition, because the identical windings are placed one on top of the other, only the d.c. voltage across the smoothing capacitors appears between winding layers and no current flows in the interlayer capacitance.

Choice of circuit for multiple-output power supplies

For instrument power supplies where a large number of different outputs are required, the flyback converter is normally the most suitable choice because it avoids the necessity of providing a large number of output chokes. Each output can be obtained from an appropriate secondary, together with a single rectifier and capacitor. The feedback voltage required to control the drive circuits can be derived from an extra winding coupled as closely as possible to the output winding requiring the best regulation.

CHOICE OF TRANSISTOR

In the foregoing section, the choice between the three main classes of converter (flyback, forward, or push-pull) was made according to the output voltage and the output ripple required from the power supply. The choice of transistor is determined mainly by the input supply voltage and the power level. In addition, the optimum operating frequency is also influenced by the input voltage, since the limitations of transistor technology dictate that the switching speeds of practical devices decrease as their voltage ratings increase.

The usual inputs to power supplies are mains, 50V d.c. in telephone systems, and 24V or 12V batteries in vehicles or portable equipment.

Operation from the mains

Transistor collector voltage

With standard mains voltages of 220 or 240V having tolerances of −20% and +10%, with 10% ripple on the rectified d.c., and with a 2V or 4V drop in the rectifier circuit, the minimum rectified voltage applied to the converter is equal to the nominal supply voltage, that is, 220 or 240V. If these minimum d.c. voltages are applied to the circuits in Fig. 7, in which previously the supply was assumed to be 200V and the losses negligible, voltage drops of 10 or 20% can be tolerated. Alternatively, where 10% is an adequate allowance for converter losses, the 10% remaining with a 240V supply allows the circuit to continue operation during a half-cycle mains drop-out.

These figures confirm that the level of 200V with no losses originally chosen for the circuits in Fig. 7 gives a realistic indication of the output power obtainable under all conditions of operation with normal mains supplies.

The same two mains voltages, 220V and 240V, taken at their maximum values of +10%, can yield maximum rectified output voltages of 340 and 370V respectively. The safe operating area graphs for power switching transistors permit collector current to flow (for specified times) with collector voltages up to but not exceeding the V_{CEO} ratings. Therefore, in Circuits 2, 4, 5 and 7 in Fig. 7, where the collector voltage can rise rapidly to that of the supply as soon as the transistor current starts to decrease, the transistors must have V_{CEO} ratings in excess of 340V for 220V mains, or 370V for 240V mains.

In Circuits 1, 3 and 6, the transistor collector voltage is permitted to rise to twice that of the supply. For these circuits, transistors with V_{CEO} ratings in excess of either 680V or 740V for the two mains voltages would be desirable. Transistors with V_{CEO} ratings in excess of these figures are, however, too slow for use in normal switched-mode power supplies because the higher voltage can only be achieved by sacrificing switching speed. The practical solution is therefore to choose a transistor having a V_{CES} rating in excess of twice the maximum supply voltage and to slow down the rise of collector voltage so that the collector current is reduced to zero before the collector voltage exceeds V_{CEO}. The additional components required to slow down the rise of collector voltage are drawn in broken line in Circuits 1, 3 and 6 in Fig. 7.

Transistor type BDY93/01, which has ratings in excess of $V_{CES} = 740V$ and $V_{CEO} = 370V$, is suitable for use in all seven converter circuits shown in Fig. 7. The voltage limiting diodes and the diodes in the slow-rise circuits should have voltage ratings equal to the $V_C$max figure of V_S or $2V_S$ for each circuit in Fig. 7. The peak current in these diodes equals the peak current in their associated transistors, but the mean current is lower and varies with the details of the particular circuit design and operation.

In special circumstances supply voltages in excess of those considered above could be accommodated using the same transistor. For example, in the flyback converter circuits, the maximum collector voltage during normal operation can be reduced by employing a transistor on-time of less than 50% and increasing the number of secondary turns to obtain the desired output voltage. This technique makes use of the basic property of the flyback converter circuit that the product of the voltage across the transformer during the transistor on-time and the 'on-time' itself equals the product of the voltage across the transformer during the off-time and the time for which that voltage exists. This method is only completely successful, however, when the leakage inductance between the primary and secondary is effectively zero, and in practice adequate damping must be employed to absorb the voltage spike that can appear at the collector when the transistor turns off. When this is achieved the bifilar winding and its diode in Circuit 1 become redundant, but of course the load on the output terminals of the power supply should not be removed. Similarly in the push-pull circuits, assuming the normal dead time between conduction of the two transistors, the voltage across the transformer secondary is locked at zero during the dead time by simultaneous conduction in both output diodes, each of which carries half the load current. Therefore, when a transistor is turned off, its collector voltage should rise to half its peak value and remain there until the next transistor is turned on, at which time the voltage should again rise to the full peak value. If this in fact occurred, the single-ended push-pull converter (Circuit 5) using the same transistor, could operate from twice the stated supply voltage. However, this only occurs in the absence of leakage inductance, and in practical cases it is possible only to minimize the leakage inductance in the transformer design and hence minimize the damping required to limit the amplitude of the voltage spikes.

Transistor collector current and switching time

The transistor peak-current of 2A used in the examples in Fig. 7 was defined as the useful current for the purpose of calculating the output power. In practice, the current would include extra components due to damping circuits and magnetizing current and therefore the value is likely to be in the region of 2·5A. The transistor must therefore be capable of switching 2·5A continuously with acceptably low switching losses. Typical switching times for the BDY93 transistor at 2·5A are 0·25μs for t_{on} and 0·4μs for t_f. These times should be as short as possible compared with the cycle time to minimize the switching losses, but the operating frequency must be kept above about 20kHz to avoid audible noise from the output transformer. At 20kHz the cycle time is 50μs, in which case t_{on} and t_f each occupy less than 1% of the available time, giving acceptably low transistor dissipation.

Therefore, a transistor such as the BDY93/01 can supply outputs in practical power supplies from 100W to 400W as shown in Fig. 7. With a larger transistor such as the BDY96 which has similar voltage ratings and appropriate switching times specified at twice the current, the output powers are doubled, giving 200 to 800W for the circuits in Fig. 7.

If a transistor is operated at peak currents higher than those at which its switching time is specified, the achievable switching times are lengthened. If it is operated at a lower peak current, the switching times are shortened. Therefore, the optimum operating frequency is reduced for higher current operation and increased for lower current operation.

The turn-off times of high voltage switching transistors are temperature dependent and are also very dependent on the base drive current waveforms employed. The design of drive circuits for this class of transistor therefore requires special attention.

Operation from lower supply voltages

All the circuits in Fig. 7 could be used on lower supply voltages but Circuits 1, 3 and 6, which operate the transistor up to twice the supply voltage, would generally be the most suitable. For a 50V nominal supply, the appropriate minimum useful supply voltage in place of the 200V shown, would be 40V, a ratio of five to one. Hence, if the previous useful peak current of 2A is increased five times to 10A, all circuits would give the powers previously indicated.

With transistors designed for operation on lower supply voltages, such as 50V and below, higher switching speeds are easily obtained, and with well designed drive circuits, turn-off times can be in the region of 0·1µs. The operating frequency of power supplies designed for lower input voltage could therefore be raised to 50kHz for example, so permitting reductions in the sizes of the output transformer and the smoothing capacitor.

Operating at a frequency of 50kHz, the cycle time would be 20µs. Therefore, as a general guide, the transistor fall-time should be in the region of 1% of 20µs, or 0·2µs. The BDY90 transistor is specified to have a fall time of less than 0·2µs at a current of 5A. Therefore, operating at 50kHz with a 'useful' peak current of 5A and a 'useful' supply voltage of 40V, the BDY90 could produce output powers equal to half those indicated in Fig. 7, giving outputs from 50W to 200W according to the circuit employed.

Using the BDY90 with a nominal 28V supply and assuming a minimum 'useful' supply voltage of 25V and a 'useful' peak current of 8A, the same product and therefore the same outputs as above are obtained. However, to counteract the increased switching losses at the higher current, the operating frequency should be reduced to about 25kHz.

In Circuits 1, 3 or 6, the maximum allowable supply voltage would be 60V, half the transistor V_{CBO} rating of 120V. In some telephone systems with nominal 50V d.c. supplies, supply line surges are permitted up to a maximum (clipped) peak value of about 70V. In such cases transistor development type 424BDY with its V_{CEO} rating of 150V may be more suitable. For this type, the switching times are specified at a peak current of 7A, so a 'useful' current of up to 5A could be employed and the output powers would again be 50W for Circuit 1, 100W for Circuit 3, and 200W for Circuit 6.

When a low power of only a few watts is required at a stabilized output voltage which is appreciably different from that of the supply, or when isolation is necessary, the switched-mode power supply principle can often be applied with advantage. For example, a BSW68 transistor having a V_{CEO} rating of 150V and a peak current rating of 2A, and operating with a 'useful' minimum supply of 40V and a 'useful' peak current of 0·5A (using these terms as earlier), would give an output of 5W in Circuit 1, 10W in Circuit 3, and 20W in Circuit 6. The 150V V_{CEO} rating would allow operation up to maximum supply of 75V.

Variable 35V 10A switched-mode voltage regulator

B. GEORGE
Mullard Central Application Laboratory

UDC 621.311.6 [621.376.5]

The design of a variable 35V 10A switching regulator working from a unregulated 40 to 50V d.c. supply is described. The circuit operates with an efficiency of ⩾ 60% at all output voltages and at currents greater than 1A.

INTRODUCTION

Switched-mode power supplies have several clear-cut advantages over conventional power supplies in many applications. For this reason, there has been extensive research and development to provide devices and circuits fully utilizing these advantages. It is hoped to publish a number of articles describing various aspects of switched-mode power supply design. Although development work is still continuing, the present article giving some of the initial Mullard work in this field, is considered to be of interest and of practical use.

The article describes the design and construction of a voltage regulator power supply using the switched-mode, or pulse-width modulation, technique. The circuit provides a continuously variable output of 5 to 35V at 0 to 10A. Before discussing the circuit, the conventional series stabilizer is described and compared with that using the switched-mode approach.

Series stabilization

One of the most common forms of stabilized power supply is that using series transistor stabilization. In such a system (Fig. 1), any change in the required output voltage V_o results in either an increase or decrease in the impedance of the series transistor which compensates for the change at the output. A constant output voltage can therefore be obtained for varying load and input voltage conditions. The unregulated input voltage must always be greater than the required d.c. output voltage.

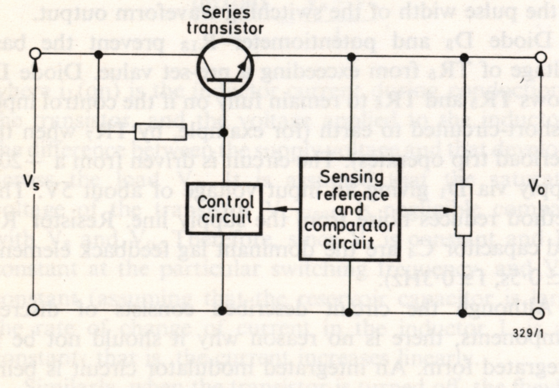

Fig. 1—Schematic diagram of simple series stabilizer

With suitable control circuits, this technique will provide a very stable and accurately controllable output voltage over a wide range of output voltages and currents. Difficulties arise, however, with high currents and low voltages. Under these conditions, the voltage drop across the series transistor becomes a significant fraction of the output voltage and cannot be reduced because of component tolerances, supply voltage variations, and supply and component impedances. High current loads consequently lead to high series-transistor dissipation which may exceed the specified maximum power ratings even though both the output current and the collector-to-emitter voltages are well within the ratings of the device. Furthermore, unless an adequate heatsink is provided, a small initial dissipation can produce a temperature rise which derates the maximum permissible dissipation and results in thermal runaway.

Good circuit design will, of course, obviate these difficulties, and careful consideration of the transistor characteristics together with the use of a large efficient heatsink, will enable the optimum circuit to be built. However, if a variable output voltage regulator is required, the resulting 'safe' circuit will often be restricted to a relatively small range of output voltages and currents, and have the additional disadvantage of requiring a large heatsink.

Switched-mode regulation

A switched-mode technique, such as pulse width modulation (or 'class D') greatly reduces the difficulties described above. Although the theory and advantages of this technique have been well known for many years, its use in practical circuits has until recently been limited by difficulties associated with the production of suitable active devices. Now, however, devices specifically designed for this mode of operation are available and the technique can be used for practical voltage regulator circuits.

The switched-mode technique is based on the principle that if the series transistor is maintained in either its fully on (bottomed) state or its cut-off state, the only dissipation occuring in the device will be that due to the output current multiplied by the $V_{CE(sat)}$ of the device. Control of the output voltage is obtained by switching the device between its on and off states at varying intervals (t_{on} and t_{off}) and the rectangular wave voltage so produced is filtered by an

LC network to give a d.c. output. Thus, the output voltage V_o is a function of the supply voltage V_s such that:

$$V_o = V_s\left(\frac{t_{on}}{t_{on}+t_{off}}\right). \qquad \ldots(1)$$

The output voltage is proportional to the duty cycle of the switching waveform. For a given duty cycle, say 1:1 (that is, with the transistor conducting for 50% of the switching period), the output voltage V_o averaged over many cycles is independent of the switching frequency. Thus, for a variable duty cycle system with a fixed or variable frequency,

$$V_o \propto \text{duty cycle.}$$

However, if the switching frequency is variable and the pulse duration (not the duty cycle) is constant, the output voltage will depend on frequency alone, that is,

$$V_o \propto \text{frequency.}$$

There are other methods of pulse modulation, such as pulse amplitude modulation (p.a.m.) and pulse phase modulation (p.p.m.), but pulse width or pulse duration modulation (p.w.m. or p.d.m.) is the one best suited to the present application.

A switched-mode voltage regulator is shown diagrammatically in Fig. 2. A variable pulse duration switching waveform is generated by the 'modulator' and is fed via a current amplifier drive circuit to the output circuit and filter network. The output voltage is sampled, and a suitable comparator circuit generates a control signal which is fed back to the modulator. Stabilization is obtained by altering the duty cycle of the switching waveform to compensate for changes in the input voltage and load at the output.

The power dissipated internally in the circuit is very small compared with that in conventional series stabilized power supplies; 20 to 30% would be a typical value.

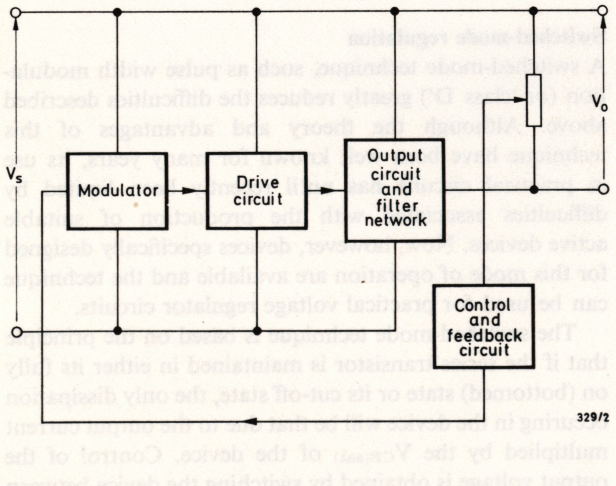
V_s
Modulator
Drive circuit
Output circuit and filter network
V_o
Control and feedback circuit
329/2

Fig. 2—Schematic diagram of switched-mode voltage regulator

However, in addition to the bottoming dissipation already mentioned, there is also some dissipation due to the edges of the switching waveform. The question of internal dissipation is discussed in detail later (see page 292).

The other major advantage of the switched-mode system is that, because of the reduced dissipation, the physical size of heatsinks can be drastically reduced. An overall packing density of 1cu.in/W (16·4ml/W) of output is not uncommon, compared with about 5 to 10cu.in/W (82 to 164ml/W) for conventional systems. There are some disadvantages with switched-mode power supplies, not the least being the problem of high frequency radiation of the fundamental and harmonics of the switching frequency. All these points will be covered in detail later.

The circuit described in this article is capable of delivering up to 10A at any voltage between 5 and 35V. The performance quoted is for the circuit driven from an unstabilized d.c. supply of about 40 to 50V. This could for example be a central battery with a nominal voltage of 50V. Alternatively, the voltage could be derived from the mains via a mains transformer and rectifier, or from a mains-to-d.c. converter.

MODULATOR

The modulator in Fig. 2 is required to generate a constant-frequency rectangular wave whose duty cycle can be varied linearly by an applied d.c. control signal. A suitable discrete circuit is shown in Fig. 3. Transistors TR_1 and TR_2 form a Schmitt trigger having upper and lower trigger levels of 1·5 and 2·0V. The squarewave output from the Schmitt trigger is applied to the base of TR_3 which, together with C_3, forms a Miller integrater. In response to the 'high' or 'low' signals from the collector of TR_2, the Miller integrator produces a triangular waveform of 0·5V peak-to-peak and 10μs duration at the collector of TR_3. This is fed back to drive the Schmitt trigger and is also applied to the base of TR_4. When the amplitude of the triangular waveform at the base of TR_4 exceeds the d.c. control voltage applied to the base of TR_5, transistor TR_4 turns off, and TR_5 and TR_6 turn on. The p.w.m. output is then low. Conversely, when the amplitude of the triangular waveform at TR_4 is less than the control voltage at TR_5, transistor TR_4 turns on, and TR_5 and TR_6 turn off. The p.w.m. output is then high. Thus, as the control voltage at the base of TR_5 changes, the duty cycle of the p.w.m. output varies accordingly. Fig. 4 shows how a change in the d.c. control voltage at the base of TR_5 results in a change in the pulse width of the switching waveform output.

Diode D_3 and potentiometer R_{13} prevent the base voltage of TR_5 from exceeding a pre-set value. Diode D_2 allows TR_5 and TR_6 to remain fully on if the control input is short-circuited to earth (for example, by TR_7 when the overload trip operates). The circuit is driven from a +20V supply via D_1 giving an input voltage of about 5V. This method reduces noise from the supply line. Resistor R_{12} and capacitor C_4 are the dominant lag feedback elements ($\tau \simeq 0{\cdot}5$s, $f \simeq 0{\cdot}3$Hz).

Although the circuit described consists of discrete components, there is no reason why it should not be in integrated form. An integrated modulator circuit is being developed.

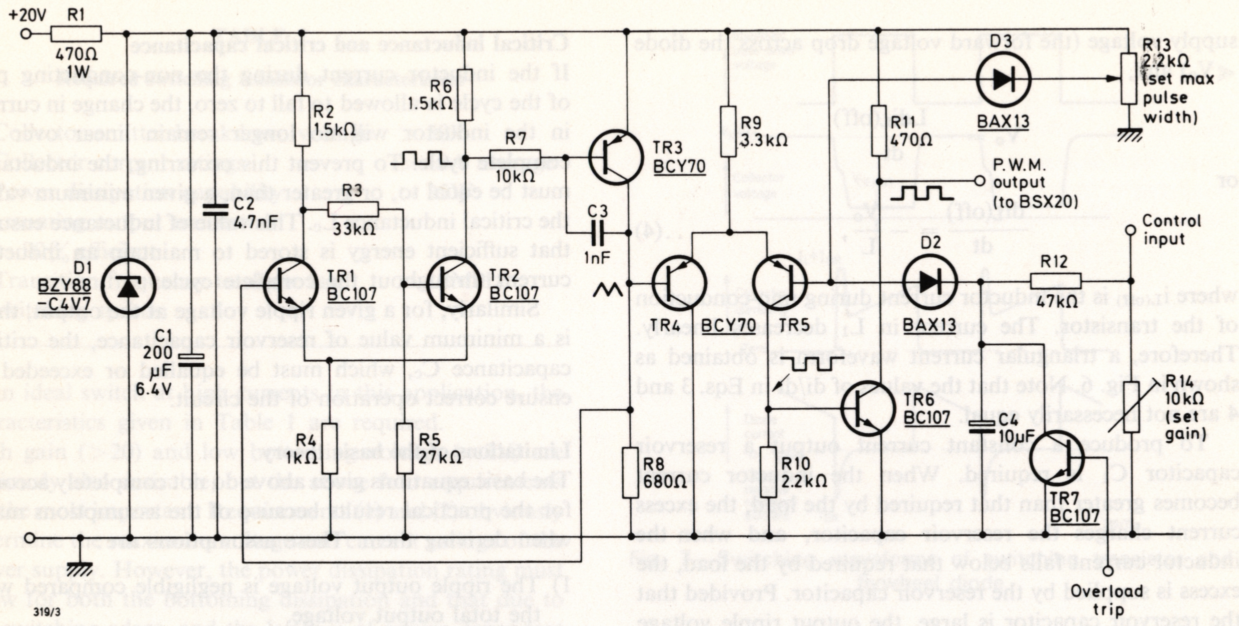

Fig. 3—Modulator circuit

OUTPUT CIRCUIT

Filter network

The modulator drives a transistor switch whose output is fed into a filter network (Fig. 5). When the transistor is conducting there is continuity through the load, filter inductance, transistor, and supply. As the transistor switch can only be in one of two states, a voltage step appears across the inductor whenever a transition from one state to the other occurs. Since,

$$E = -L\frac{di}{dt}, \qquad \ldots(2)$$

it follows that in the on-state,

$$V_s - V_o = \frac{L\,di_L(on)}{dt},$$

or

$$\frac{di_L(on)}{dt} = \frac{V_s - V_o}{L}, \qquad \ldots(3)$$

where i_L(on) is the inductor current during conduction of the transistor, and the voltage applied to the inductor is the difference between the supply voltage and that developed across the load V_o. It is assumed that the saturation voltage of the transistor $V_{CE(sat)}$ is negligible compared with V_s and V_o. Therefore, since V_s is constant and L is constant at the particular switching frequency, and V_o is constant (assuming that the reservoir capacitor is large), the rate of change of current in the inductor L is also constant; that is, the current increases linearly.

Similarly, when the transistor is turned off, the flywheel diode D_1 clamps the collector voltage at approximately the

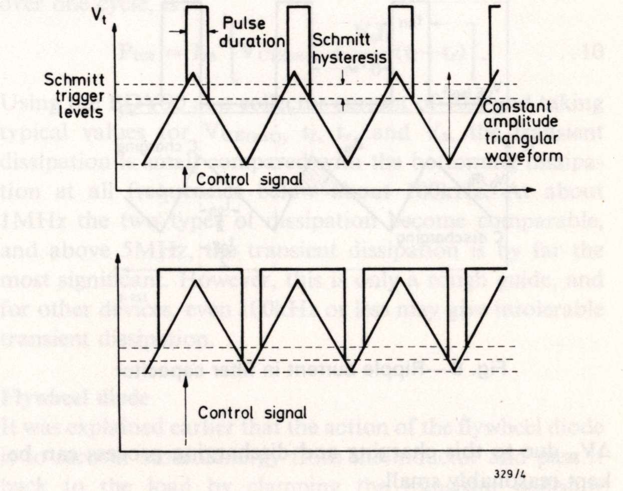

Fig. 4—Effect of change in d.c. control voltage on pulse duration of switching waveform

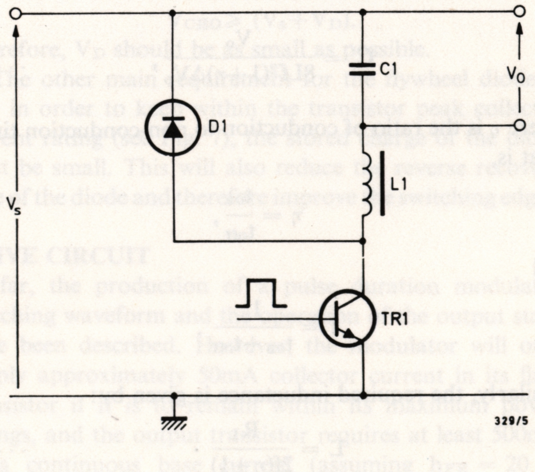

Fig. 5—Basic filter network

supply voltage (the forward voltage drop across the diode $\ll V_o$) and,

$$V_o = -\frac{L\,di_L(\text{off})}{dt}$$

or

$$\frac{di_L(\text{off})}{dt} = -\frac{V_o}{L}, \qquad \ldots(4)$$

where $i_{L(\text{off})}$ is the inductor current during non-conduction of the transistor. The current in L_1 decreases linearly. Therefore, a triangular current waveform is obtained as shown in Fig. 6. Note that the values of di/dt in Eqs. 3 and 4 are not necessarily equal.

To produce a constant current output a reservoir capacitor C_1 is required. When the inductor current becomes greater than that required by the load, the excess current charges the reservoir capacitor, and when the inductor current falls below that required by the load, the excess is supplied by the reservoir capacitor. Provided that the reservoir capacitor is large, the output ripple voltage ΔV_o due to this charging and discharging process can be kept reasonably small.

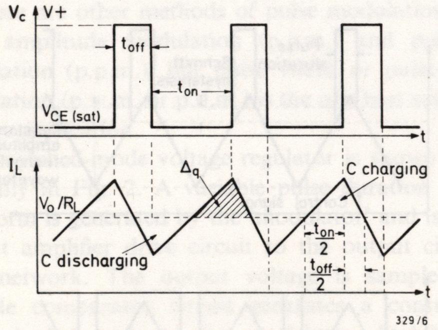

Fig. 6—Ripple current in filter capacitor

It can be shown (see Appendix 1) that for a given ripple output voltage ΔV_o, and output voltage V_o, a switching frequency f, and an inductance L, the required reservoir capacitance is given by:

$$C = \frac{V_o}{8Lf^2(1+\eta)\Delta V_o}, \qquad \ldots(5)$$

where η is the ratio of conduction to non-conduction time. That is,

$$\eta = \frac{t_{on}}{t_{off}},$$

and

$$f = \frac{1}{t_{on}+t_{off}}.$$

Similarly, the required inductance is given by:

$$L = \frac{R_L}{2f(\eta+1)}. \qquad \ldots(6)$$

Critical inductance and critical capacitance

If the inductor current during the non-conducting part of the cycle is allowed to fall to zero, the change in current in the inductor will no longer remain linear over the complete cycle. To prevent this occurring, the inductance must be equal to, or greater than, a given minimum value, the critical inductance L_c. This value of inductance ensures that sufficient energy is stored to maintain an inductive current throughout the complete cycle.

Similarly, for a given ripple voltage at the output, there is a minimum value of reservoir capacitance, the critical capacitance C_c, which must be equalled or exceeded to ensure correct operation of the circuit.

Limitations of the basic theory

The basic equations given above do not completely account for the practical results because of the assumptions made when deriving them. These assumptions are:

1) The ripple output voltage is negligible compared with the total output voltage.
2) The capacitance is ideal; that is, it has zero series resistance and inductance.
3) The inductor is a pure inductor; that is, it has no resistive or capacitive components.

Assumption (2) has quite noticeable limitations. The series resistance of a large capacitor used as a reservoir at the output of the power supply can be 200mΩ or more. Further, if the power supply is providing an output voltage of 20V, the typical peak-to-peak current charging and discharging the reservoir capacitor is approximately 0·5A. Thus, if the series resistance is 100mΩ, a voltage change of 50mV is generated across the capacitor, and therefore across the load, which is in addition to the calculated output voltage ripple. If the design assumes a ripple of 100mV peak-to-peak, this extra term amounts to a 50% increase.

The only method of reducing the ripple voltage without including further LC smoothing stages is to use a number of smaller value capacitors in parallel. The capacitances are additive, giving the required capacitance value, but the effective series resistance R_{eff} is:

$$R_{eff} = \frac{R_s}{n}, \qquad \ldots(7)$$

where n is the number of similar parallel capacitors used, each having a series resistance R_s. If ten similar capacitors replace one large one, the effective series resistance, and therefore the additional output ripple, is reduced by a factor of ten. In fact, this factor may be somewhat larger because in practice a smaller value capacitor usually has a lower series resistance. However, the increase in physical size associated with the additional components can be quite substantial, despite the reduction in size of the individual capacitors.

Switching transistor

The characteristics of the switching device are of fundamental importance to the operation of the circuit. The need for good performance in many parameters makes the fabrication of the device very difficult and as usual necessitates a compromise. For the transistor to approximate to an ideal switch at high currents in this application, the characteristics given in Table 1 are required.

TABLE 1

Required switching transistor characteristics

1) Collector-emitter breakdown voltage	> 50V
2) Collector current ratings	> 10A average
3) Power dissipation capability assuming output transistors > 90% efficient	> 35W
4) Transition frequency to allow fast switching speeds	> 10MHz

High gain (>20) and low bottoming voltage (<2V) are obviously also desirable, but the above four requirements are the most important. Requirements (1) and (2) obviously determine the maximum voltage and current ratings of the power supply. However, the power dissipation rating must allow for both the bottoming dissipation and that due to the switching edges, and the latter is of course dependent on the f_T of the device. For the present application, the BDY90 is an ideal transistor. This device has a V_{CEO} rating of 100V and a maximum collector current I_{CM}max of 15A. It also has an f_T of 70MHz(typ) which allows the regulator to operate at a switching frequency of 100kHz with minimal edge dissipation.

In addition to the continuous current rating, the peak current rating I_{CM}max is also critical because, when the transistor turns on, it has initially to carry both the inductor current I_L and also the reverse current I_{DR} from the flywheel diode (D_1 in Fig. 5) when this is reverse-biased. Fig. 7 shows typical transistor and flywheel diode switching waveforms.

Power dissipation in the transistor

Power dissipation in the output transistor can be broken down into two main parts; that due to $V_{CE(sat)}$ and that due to the dissipation in the transient switching edges.

As the pulse width is variable from about 0 to 95% of the total period, the worst-case dissipation due to the bottoming voltage is at maximum pulse width. Therefore, the average dissipation over a complete cycle is in the worst case:

$$P_{s(av)} = V_{CE(sat)} \times I_m \times \frac{95}{100} \simeq V_{CE(sat)} \times I_m, \qquad \ldots(8)$$

where I_m is the maximum (continuous) collector current.

The transient dissipation is directly proportional to switching frequency. At a frequency f_s the average transient dissipation $P_{t(av)}$ can be shown (see Appendix 2) to be:

$$P_{t(av)} = \frac{V_s I_m}{6}(t_f+t_r)f_s, \qquad \ldots(9)$$

where t_r and t_f are the rise and fall times.

Thus,

$$P_{t(av)} \propto f_s.$$

Eq. 9 assumes that:

1) The leading and trailing edges rise and fall linearly with time.
2) The V_{CEsat} is negligible compared with the supply voltage V_s, that is, $V_{CE(sat)} \ll V_s$.

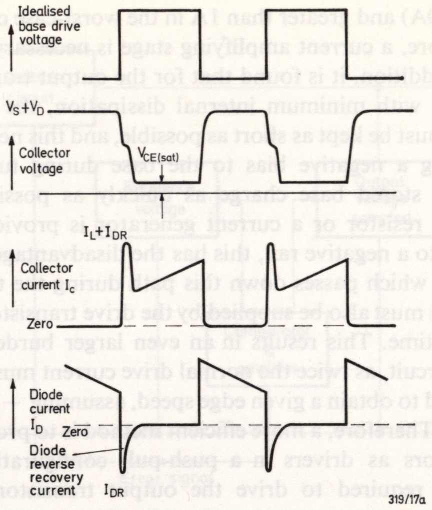

Fig. 7—Switching waveforms of switching transistor and flywheel diode

These assumptions are reasonable and give a sufficiently accurate value of power dissipation for most purposes. Thus, the total power dissipation in the device, averaged over one cycle, is:

$$P_{tot} = I_m\left[V_{CE(sat)} + \frac{V_s f_s}{6}(t_f+t_r)\right]. \qquad \ldots 10$$

Using the BDY90 at a collector current of 10A and taking typical values for $V_{CE(sat)}$, t_f, t_r, and V_s, the transient dissipation is small compared with the bottoming dissipation at all frequencies below about 100kHz. At about 1MHz the two types of dissipation become comparable, and above 5MHz, the transient dissipation is by far the most significant. However, this is only a rough guide, and for other devices, even 100kHz or less may give intolerable transient dissipation.

Flywheel diode

It was explained earlier that the action of the flywheel diode is to recover stored energy from the inductor and pass it back to the load by clamping the transistor collector voltage at approximately the supply voltage. However, the collector voltage will only be limited to the supply voltage if the forward voltage drop of the diode V_D is small, and it should be noted that for the transistor:

$$V_{CEO} \geqslant (V_s+V_D).$$

Therefore, V_D should be as small as possible.

The other main requirement for the flywheel diode is that in order to keep within the transistor peak collector current rating (see Fig. 7), the stored charge of the diode must be small. This will also reduce the reverse recovery time of the diode and therefore improve the switching edges.

DRIVE CIRCUIT

So far, the production of a pulse duration modulated switching waveform and the operation of the output stage have been described. However, the modulator will only supply approximately 50mA collector current in its final transistor if it is to remain within its maximum power ratings, and the output transistor requires at least 500mA as a continuous base current (assuming $h_{FE} = 20$ at

I_c = 10A) and greater than 1A in the worst-case condition. Therefore, a current amplifying stage is necessary.

In addition, it is found that for the output transistor to operate with minimum internal dissipation, the transient edges must be kept as short as possible, and this necessitates applying a negative bias to the base during turn-off to remove stored base charge as quickly as possible. If a leakage resistor or a current generator is provided, connected to a negative rail, this has the disadvantage that the current which passes down this path during the transistor off-time must also be supplied by the drive transistor during the on-time. This results in an even larger burden on the drive circuit, as twice the normal drive current must now be supplied to obtain a given edge speed, assuming $-I_b(\text{on}) = I_b(\text{off})$. Therefore, a more efficient method is to provide two transistors as drivers in a push-pull configuration. The current required to drive the output transistor is then halved.

Again, there are two possibilities; either two similar drive transistors can be switched in antiphase, or a complementary pair of drive transistors can be driven from a single-phase source. Examples of both these types of drive circuit are shown in Figs. 8a and 8b.

Difficulties arise with the first method because a phase inversion usually requires one or more additional transistors, and interaction can occur between the drive transistors which are working in opposition. The complementary pair circuit overcomes this difficulty by using a single-phase drive. However, this system still uses a constant voltage drive which presents problems from switching transients. Inductive transient voltages developed in the emitter lead of the output transistor when the transistor is turned on can be very large, particularly when the lead length of this connection cannot be kept short. With an edge speed of 100ns and a current of 10A switched through an inductance of approximately 60nH (equivalent to a lead length of about 50mm), the induced voltage transient will be approximately 6V.

This can be sufficient to effectively turn off the drive before the output transistor has properly turned on, and thus an oscillatory effect occurs whereby the output turns on and off many times in rapid succession. This leads to greatly increased transistor dissipation because of the increased number of switching edges (see Fig. 9).

To reduce this effect, a current source may be provided to maintain the drive current, even under transient conditions. However, even here there is a risk of the current source being cut off unless it is supplied from a sufficiently high potential. The actual circuit used is shown in Fig. 10, and this provides an adequate drive current for most reasonable emitter lead lengths (up to about 50mm). Longer lead lengths can be tolerated using a higher supply line voltage but with higher dissipation.

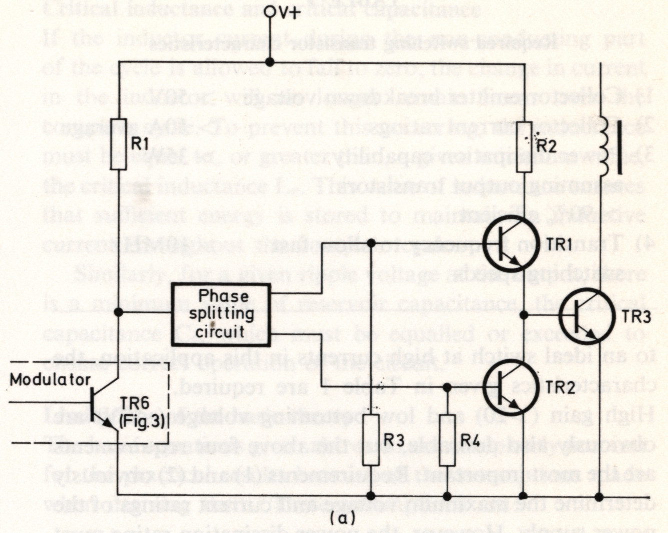

Fig. 8a—Two drive transistors switched in antiphase

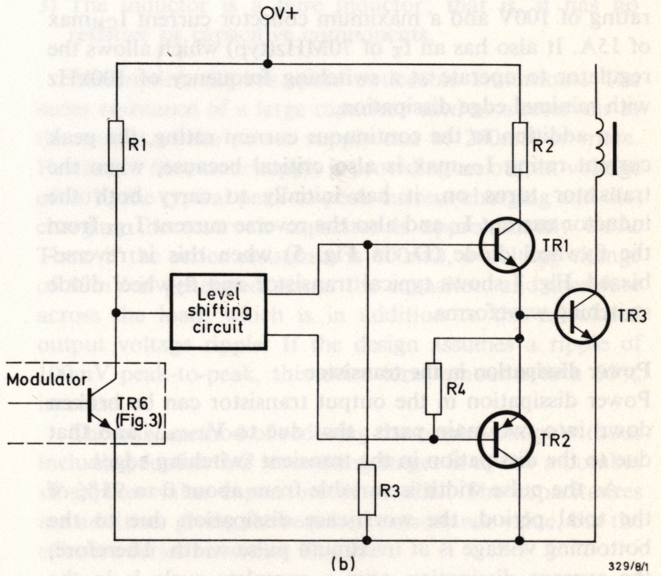

Fig. 8b—Complementary drive transistors switched from a single-phase source

The drive current I_d is set by the voltage regulator diode D_1 and the resistor R_3 such that when TR_2 is turned on,

$$I_d = \frac{V_{D1} - V_{BE2}}{R_3}.$$

where V_{BE2} is the base-emitter voltage of TR_2 at the particular emitter current. It should be noted that TR_2 carries the drive current in addition to dropping a large proportion of the drive line voltage. Therefore, a large dissipation rating will be required for this device, and the situation is worsened when running from a higher supply line voltage.

When TR_2 is turned off, the output transistor TR_4 is pulled off by the negative supply voltage through TR_3, the reverse base current of TR_4 being limited by R_5. Thus a controlled turn-off characteristic is obtained, and to assist in keeping the turn-off as short as possible, TR_4 is held out of saturation during its conduction time by anti-saturation diodes D_2 and D_3. This improves the switching edges, although it does result in a greater output transistor dissipation.

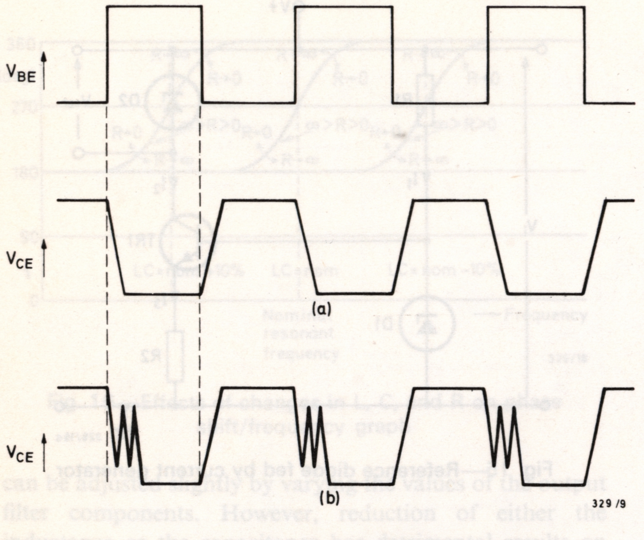

Fig. 9—Comparison of switching waveforms
(a) collector voltage with adequate drive
(b) collector voltage with inadequate drive

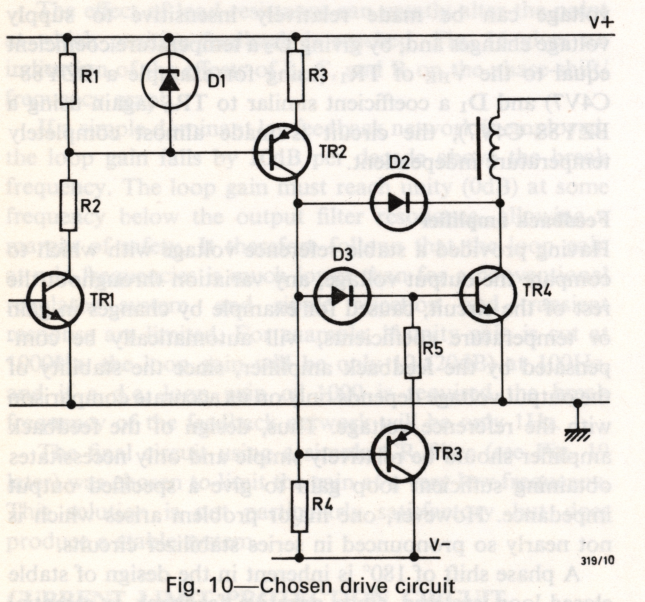

Fig. 10—Chosen drive circuit

CONTROL CIRCUIT

To produce a stabilized voltage output from the power supply, it is necessary to provide a feedback path so that the duty cycle of the switching waveform can be adjusted by the modulator according to the requirements of the output. This is shown diagrammatically in Fig. 11. The output voltage is monitored, and compared with a fixed reference voltage. The error signal so produced is fed back to the modulator to cause the duty cycle of the switching waveform to increase or decrease depending on whether the output voltage is too low or too high.

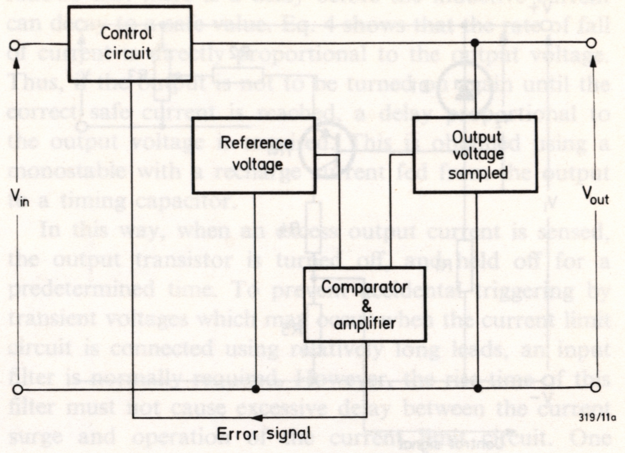

Fig. 11—Control loop

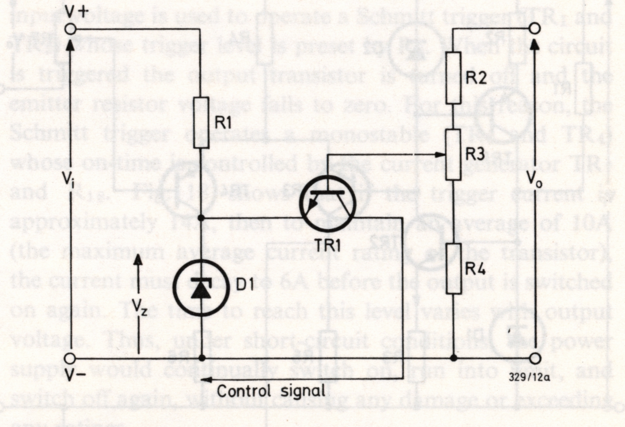

Fig. 12—Simple comparator circuit

Comparator

A comparator circuit usually consists of one or more active devices and compares the reference voltage and sampled voltage, while simultaneously amplifying the error signal to a value more suitable for the feedback circuits. A typical circuit is shown in Fig. 12. The reference voltage on the emitter of the comparator transistor TR_1 is set so that there is equilibrium when the potential at the base is $(V_Z + V_{BE})$. The base-emitter voltage V_{BE} is that necessary to provide sufficient output current from the collector to drive the modulator. The circuit can be made relatively insensitive to temperature changes by arranging for the zener voltage of the voltage regulator diode D_1 and the V_{BE} of the transistor to have equal and opposite temperature coefficients. However, this simple circuit cannot be used directly in the switched-mode power supply because, as can be seen from Fig. 2, the output voltage is not referenced to the same earth as the input. The only common rail between supply voltage and output voltage is the positive supply line. Therefore, the circuit of Fig. 13 in which V_z is referenced to the supply line and the control signal is referenced to the earth line of the modulator can be adopted. When this circuit is in a stable state,

$$V_{ref} = V_{BE} + \Delta V_o.$$

Thus, a change in V_{BE} caused by a change in temperature will have a direct effect on the effective reference voltage unless the temperature coefficient of the regulator diode zener voltage and the transistor V_{BE} are made equal. This can prove difficult in practice and so a more suitable

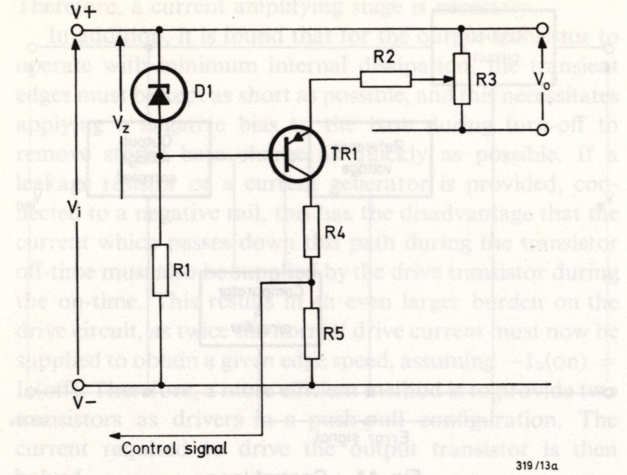

Fig. 13—Comparator circuit with V_Z referenced to supply line

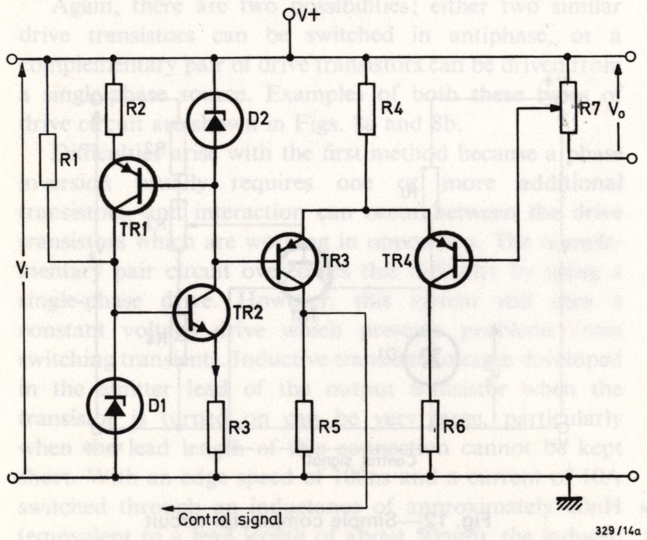

Fig. 14—Comparator circuit using long-tail pair

comparator is the long-tail pair circuit shown in Fig. 14. Now, provided that the transistors are similar (preferably matched), their temperature coefficients of V_{BE} will compensate each other. It is then only necessary to choose a voltage regulator diode with zero temperature coefficient.

Reference voltage

The zener voltage of the voltage regulator diode can vary both because of temperature changes and changes in supply voltage. The former can be compensated either by choosing a regulator diode with a low temperature coefficient or by using a regulator diode and forward biased diode in series so that the overall temperature coefficient is zero; that is, the coefficients are equal and opposite.

Variations in reference voltage due to supply changes are not quite so easy to control. The variation in voltage is caused by a change in current through the regulator diode which is most noticeable when the diode is fed from a voltage source in series with a resistor. The most effective way of reducing this change in current is to feed the diode from a current generator as shown in Fig. 15. The current generator is also referenced to a voltage regulator diode but the change in reference voltage (D_2 in Fig. 15) due to supply voltage changes is now reduced by a factor of 10^5.

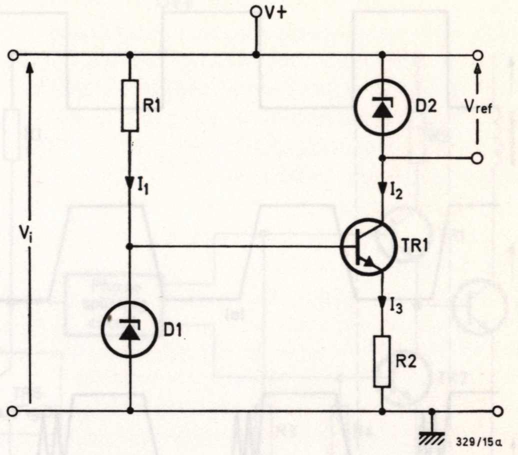

Fig. 15—Reference diode fed by current generator

This can be further reduced by supplying D_1 from a current generator derived from the stable voltage of D_2. Thus the final circuit is as shown in Fig. 14. The reference voltage can be made relatively insensitive to supply voltage changes and, by giving D_2 a temperature coefficient equal to the V_{BE} of TR_1 (using for example a BZY88–C4V7) and D_1 a coefficient similar to TR_2 (again using a BZY88–C4V7), the circuit is made almost completely temperature independent.

Feedback amplifier

Having provided a stable reference voltage with which to compare the output voltage, any variation throughout the rest of the circuit, caused for example by changes in gain or temperature coefficients, will automatically be compensated by the feedback amplifier, since the stability of the output voltage depends only on its accurate comparison with the reference voltage. Thus, design of the feedback amplifier should be relatively simple and only necessitates obtaining sufficient loop gain to give a specified output impedance. However, one major problem arises which is not nearly so pronounced in series stabilizer circuits.

A phase shift of 180° is inherent in the design of stable closed-loop systems, since negative feedback is essential to maintain d.c. stability. However, the output filter of the power supply consists of inductive and capacitive components (see Fig. 5) required to convert the switched source into a d.c. output. This LC filter gives rise to an additional phase shift of 180° at some frequency determined by the resonance of the filter and the damping factor of the load resistance. Thus, at the resonant frequency of the filter, at least a further 90° phase shift is experienced, giving a loop phase shift of 270°. To ensure stability, it is essential to reduce the loop gain to less than unity before the loop phase shift reaches 360° (that is, positive feedback). In series stabilizer circuits employing LC filters at the output, this problem is usually not too critical because the resonant frequency is reasonably high. However, in this application, the component values must be relatively large to provide adequate filtering, and so resonance occurs at a much lower frequency, typically 2·8kHz.

The actual frequency at which this effect takes place can be adjusted slightly by varying the values of the output filter components. However, reduction of either the inductance or the capacitance has detrimental results on other factors in the performance of the supply, such as output ripple voltage (at the switching frequency). Therefore, any compromise is somewhat unsatisfactory.

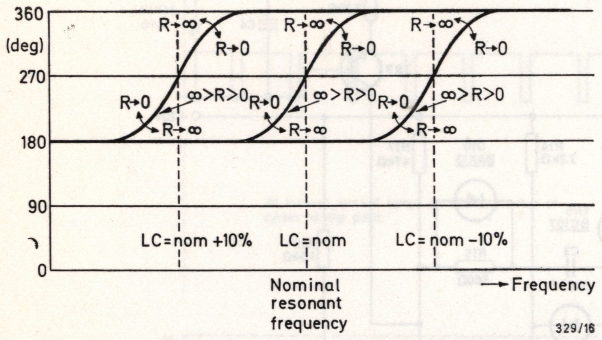

Fig. 16—Effects of changes in L, C, and R on phase shift/frequency graph

The effect of load resistance can greatly alter the point at which positive feedback is reached. Fig. 16 gives an indication of the effects of L, C, and R on the phase-shift/frequency graph.

If a simple dominant lag feedback network is employed, the loop gain falls by 20dB per decade above the break frequency. The loop gain must reach unity (0dB) at some frequency below the output filter resonance, allowing a margin of safety. It therefore follows that the loop gain at mid-frequencies is much lower than for a conventional regulator system, and ripple rejection and transient response are limited. For example, if unity gain is cut at 1000Hz, the loop gain will be only 10 (20dB) at 100Hz, and if a d.c. loop gain of 1000 is required the break frequency of the feedback network will be only 1Hz.

The final circuit using a simple CR filter (see Fig. 19 later) was chosen to limit the gain at a very low frequency. This solution is not particularly satisfactory but does produce a stable system.

CURRENT LIMIT PROTECTION CIRCUIT

Some method of current limiting is necessary both to protect the power supply from excessive output currents (short circuited output) and also to prevent excessive currents during turn-on when all the capacitors are discharged. The most vulnerable element in the supply is the switching transistor, and so to limit the collector (or emitter) current to a safe value inside the maximum specified ratings, it is necessary to monitor the transistor current. This is achieved using an emitter resistor. Provided that this is small in value, the drive conditions of the output transistor are not upset and the resistor dissipation is kept moderately low. A 50mΩ resistor will drop only 500mV at 10A emitter current and will dissipate 5W.

The operation of the current limit circuit is as follows. Once excessive current has been sensed, the output transistor is immediately turned off. This is done most easily by turning off the pulse width modulator. As the rate of rise or fall of inductor current is approximately linear, it follows that there is a delay before the inductive current can decay to a safe value. Eq. 4 shows that the rate of fall of current is directly proportional to the output voltage. Thus, if the output is not to be turned on again until the correct safe current is reached, a delay proportional to the output voltage is required. This is obtained using a monostable with a recharge current fed from the output to a timing capacitor.

In this way, when an excess output current is sensed, the output transistor is turned off, and held off for a predetermined time. To prevent accidental triggering by transient voltages which may occur when the current limit circuit is connected using relatively long leads, an input filter is normally required. However, the rise-time of this filter must not cause excessive delay between the current surge and operation of the current limit circuit. One saving factor is that the limited rise-time of the collector current ensures that even under short-circuit conditions the increase in current is carefully controlled.

Fig. 17 shows the complete current limit circuit. The input voltage is used to operate a Schmitt trigger (TR_1 and TR_2) whose trigger level is preset by R_8. When the circuit is triggered the output transistor is turned off and the emitter resistor voltage falls to zero. For this reason, the Schmitt trigger operates a monostable (TR_3 and TR_4) whose on-time is controlled by the current generator TR_7 and R_{18}. Fig. 18 shows that if the trigger current is approximately 14A, then to maintain an average of 10A (the maximum average current rating of the transistor), the current must decay to 6A before the output is switched on again. The time to reach this level varies with output voltage. Thus, under short-circuit conditions, the power supply would continually switch on, run into limit, and switch off again, without causing any damage or exceeding any ratings.

Finally, the output of the monostable directly drives the input to the pulse width modulator (TR_7 in Fig. 3). The various catching diodes employed in the circuit ensure that the limit operates as fast as possible once the trigger condition has been sensed.

VOLTAGE REGULATOR CIRCUIT AND PERFORMANCE

The complete circuit of the regulator is shown in Figs. 19a and 19b. The numbers to the right of Fig. 19a and to the left of Fig. 19b indicate how the two halves of the circuit are connected. The positive supplies, +8V and +20V, could be derived directly from the +50V supply. The −6V supply could be obtained from a small auxiliary switched-mode supply. Alternatively, the supplies can be derived from the mains using a transformer and rectification. The devices shown in Fig. 19 are the ones which were actually used in the prototype circuit, and have been retained to allow performance measurements to be quoted. However, new devices are constantly being developed and the most recent Mullard product lists should always be consulted before constructing any circuit.

A summary of the regulator performance is given in Table 2. For convenience, measurements were taken with the circuit driven from an unstabilized d.c. supply.

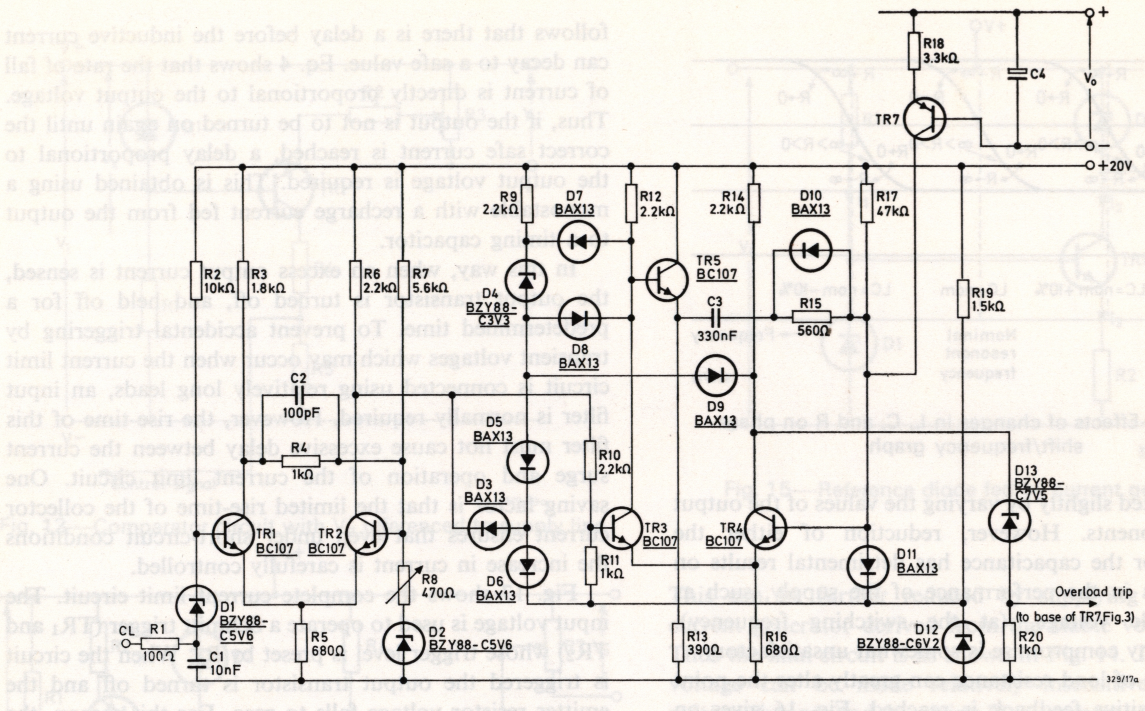
R18 3.3kΩ
C4
V_o
TR7
+
−
+20V
R9 2.2kΩ
D7 BAX13
R12 2.2kΩ
R14 2.2kΩ
D10 BAX13
R17 47kΩ
R2 10kΩ
R3 1.8kΩ
R6 2.2kΩ
R7 5.6kΩ
D4 BZY88-C3V3
D8 BAX13
TR5 BC107
C3 330nF
R15 560Ω
R19 1.5kΩ
C2 100pF
R4 1kΩ
D5 BAX13
D9 BAX13
R10 2.2kΩ
D3 BAX13
D13 BZY88-C7V5
TR1 BC107
TR2 BC107
TR3 BC107
TR4 BC107
R11 1kΩ
D11 BAX13
D6 BAX13
R8 470Ω
D1 BZY88-C5V6
CL
R1 100Ω
C1 10nF
R5 680Ω
D2 BZY88-C5V6
R13 390Ω
R16 680Ω
D12 BZY88-C6V2
R20 1kΩ
Overload trip (to base of TR7,Fig.3)
329/17a

Fig. 17—Current limit circuit

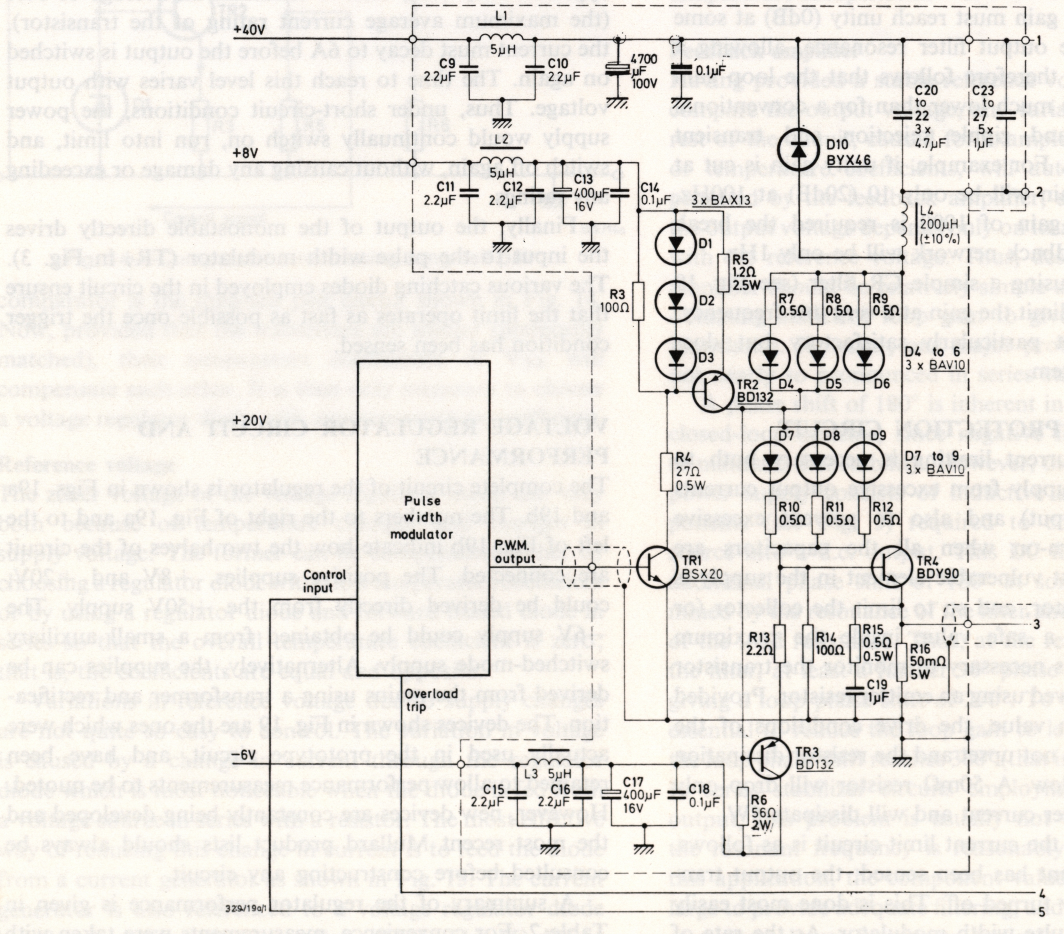
+40V
L1 5µH
C9 2.2µF
C10 2.2µF
4700µF 100V
0.1µF
C20 to 22 3x 4.7µF
C23 to 27 5x 1µF
L2 5µH
D10 BYX46
+8V
C11 2.2µF
C12 2.2µF
C13 400µF 16V
C14 0.1µF
3 x BAX13
L4 200µH (±10%)
D1
D2
D3
R3 100Ω
R5 1.2Ω 2.5W
R7 0.5Ω
R8 0.5Ω
R9 0.5Ω
D4 to D6 3 x BAV10
TR2 BD132
+20V
Pulse width modulator
P.W.M. output
Control input
R4 27Ω 0.5W
D7 to D9 3 x BAV10
R10 0.5Ω
R11 0.5Ω
R12 0.5Ω
TR1 BSX20
TR4 BDY90
R13 2.2Ω
R14 100Ω
R15 0.5Ω 5W
R16 50mΩ 5W
C19 1µF
Overload trip
−6V
L3 5µH
C15 2.2µF
C16 2.2µF
C17 400µF 16V
C18 0.1µF
TR3 BD132
R6 56Ω 2W
1
2
3
4
5
329/19a

Fig. 19a—Voltage regulator circuit

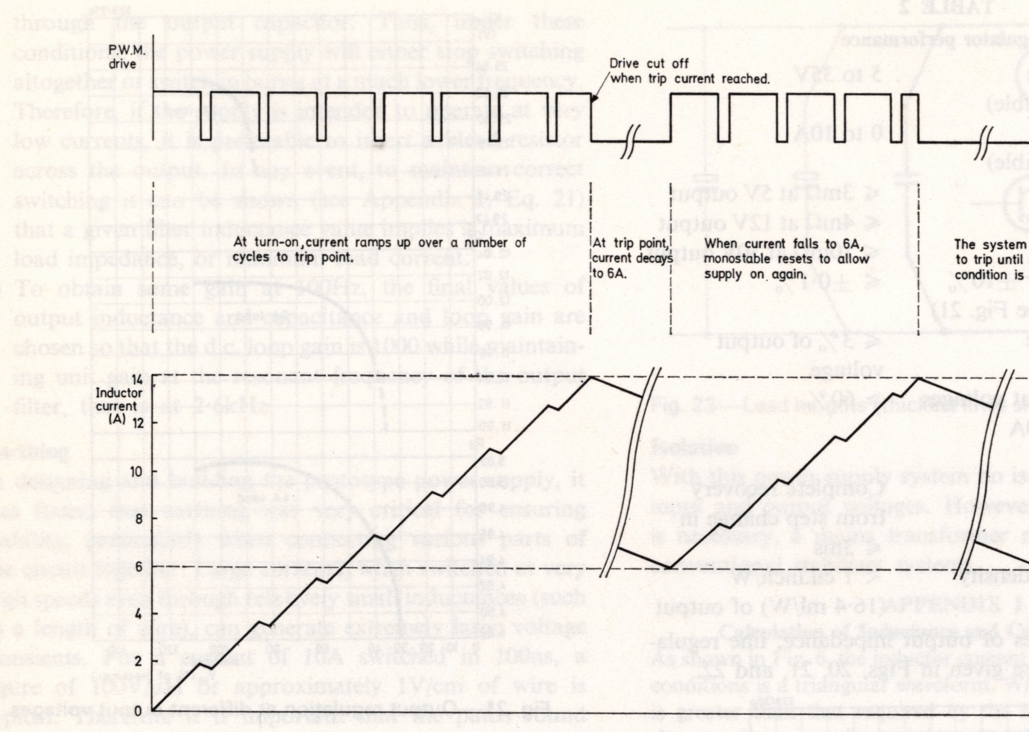

Fig. 18—Operation of current limit under short-circuit conditions

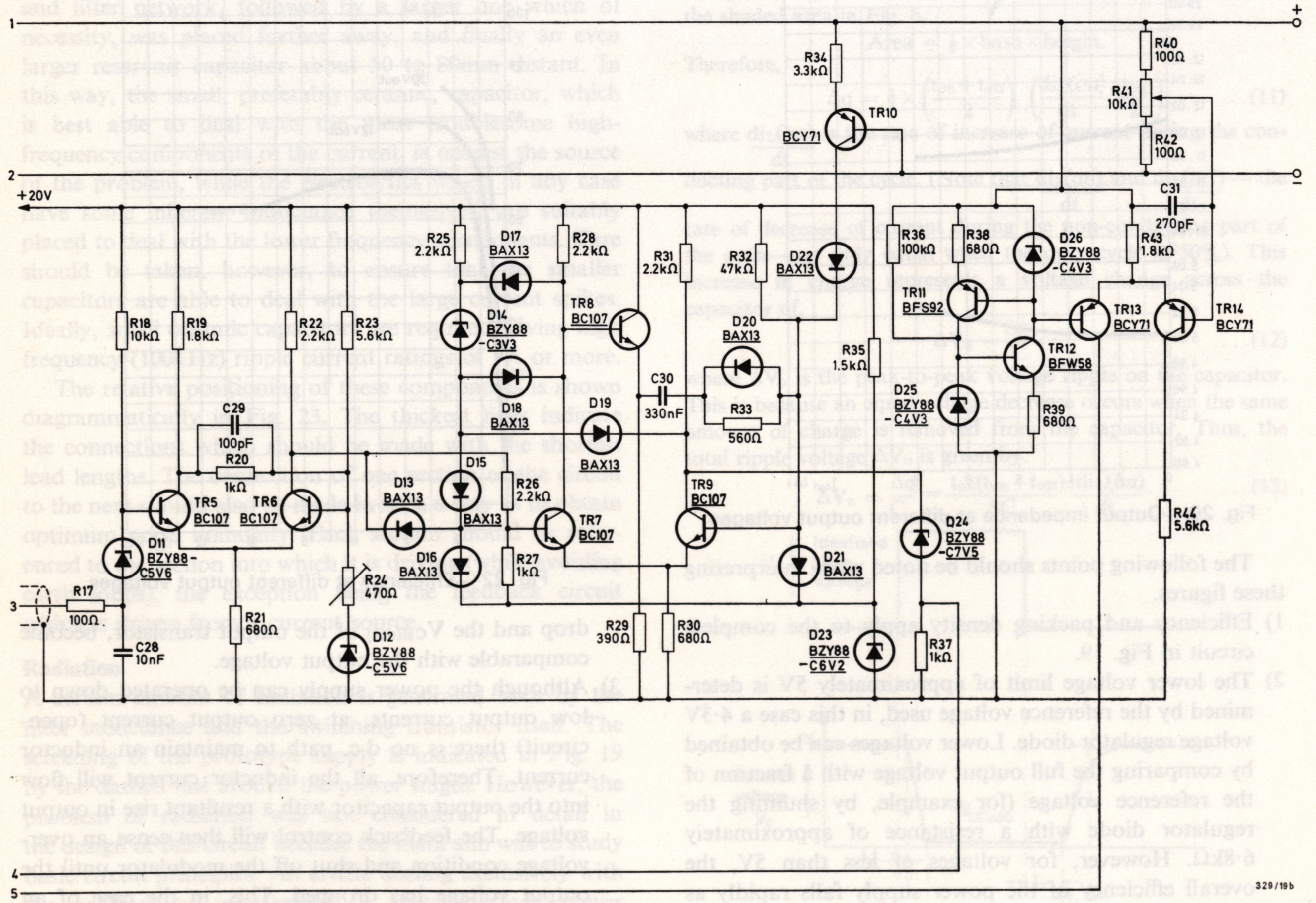
1
2
3
4
5
+
−
+20V
R34 3.3kΩ
R40 100Ω
R41 10kΩ
R42 100Ω
TR10 BCY71
C31 270pF
R25 2.2kΩ
D17 BAX13
R28 2.2kΩ
R31 2.2kΩ
R32 47kΩ
D22 BAX13
R36 100kΩ
R38 680Ω
D26 BZY88-C4V3
R43 1.8kΩ
TR8 BC107
TR11 BFS92
TR13 BCY71
TR14 BCY71
R18 10kΩ
R19 1.8kΩ
R22 2.2kΩ
R23 5.6kΩ
D14 BZY88-C3V3
D18 BAX13
D20 BAX13
R35 1.5kΩ
R33 560Ω
TR12 BFW58
D25 BZY88-C4V3
R39 680Ω
C29 100pF
R20 1kΩ
D19 BAX13
C30 330nF
TR5 BC107
TR6 BC107
D13 BAX13
D15 BAX13
R26 2.2kΩ
D16 BAX13
TR7 BC107
TR9 BC107
D24 BZY88-C7V5
R27 1kΩ
D11 BZY88-C5V6
R24 470Ω
D21 BAX13
R17 100Ω
R21 680Ω
C28 10nF
D12 BZY88-C5V6
R29 390Ω
R30 680Ω
D23 BZY88-C6V2
R37 1kΩ
R44 5.6kΩ
329/19b

Fig. 19b—Voltage regulator circuit (contd)

TABLE 2

Regulator performance

Output voltage range (continuously variable)	5 to 35V
Output current (continuously variable)	0 to 10A
Output impedance (see Fig. 20)	⩽ 3mΩ at 5V output ⩽ 4mΩ at 12V output ⩽ 10mΩ at 30V output
Output regulation for ±10% mains variation (see Fig. 21)	⩽ ±0·1%
Output ripple voltage (peak-to-peak)	⩽ 3% of output voltage
Efficiency at all output voltages and currents ≻ 1·0A (see Fig. 22)	⩾ 60%
Transient response	Complete recovery from step change in ⩽ 3ms
Component packing density	< 1 cu.inch/W (16·4 ml/W) of output

Performance curves of output impedance, line regulation, and efficiency are given in Figs. 20, 21, and 22.

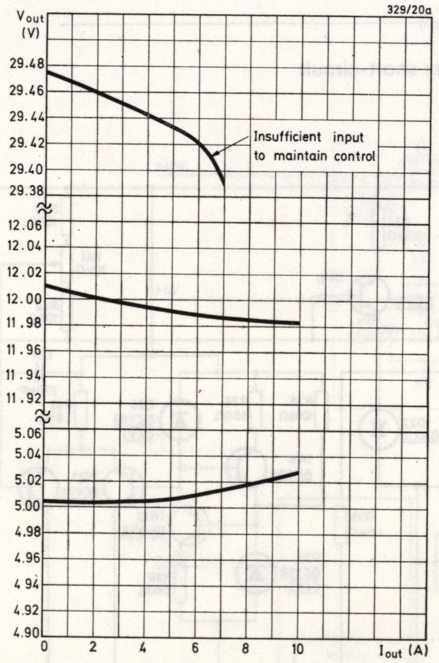

Fig. 20—Output impedance at different output voltages

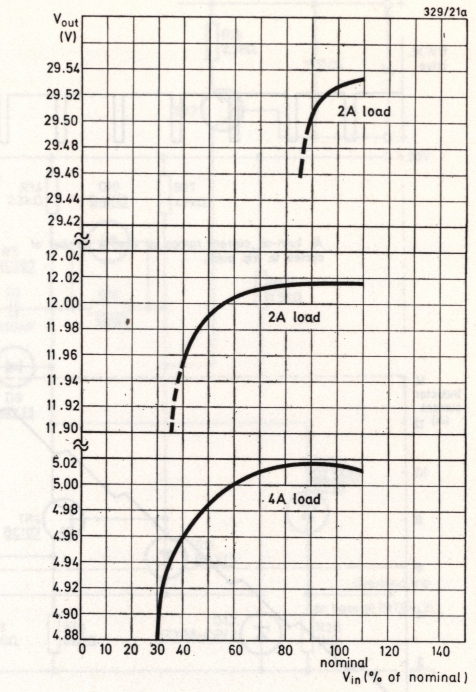

Fig. 21—Output regulation at different output voltages

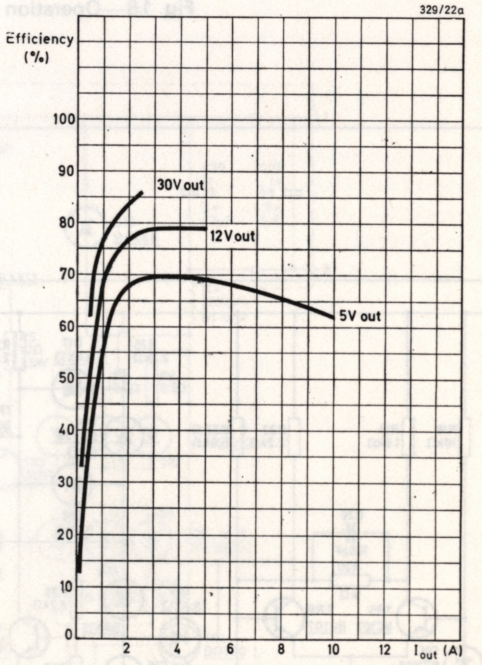

Fig. 22—Efficiency at different output voltages

The following points should be noted when interpreting these figures.

1) Efficiency and packing density apply to the complete circuit in Fig. 19.
2) The lower voltage limit of approximately 5V is determined by the reference voltage used, in this case a 4·3V voltage regulator diode. Lower voltages can be obtained by comparing the full output voltage with a fraction of the reference voltage (for example, by shunting the regulator diode with a resistance of approximately 6·8kΩ. However, for voltages of less than 5V, the overall efficiency of the power supply falls rapidly as the voltage losses, such as the flywheel diode voltage drop and the $V_{CE(sat)}$ of the output transistor, become comparable with the output voltage.
3) Although the power supply can be operated down to low output currents, at zero output current (open-circuit) there is no d.c. path to maintain an inductor current. Therefore, all the inductor current will flow into the output capacitor with a resultant rise in output voltage. The feedback control will then sense an over-voltage condition and shut off the modulator until the output voltage has dropped. This, in the case of an open-circuit output, depends on the leakage current through the output capacitor. Thus, under these conditions, the power supply will either stop switching altogether or switch in bursts at a much lower frequency. Therefore, if the supply is intended to operate at very low currents, it is preferable to insert a bleed resistor across the output. In any event, to maintain correct switching it can be shown (see Appendix 1, Eq. 21) that a given filter inductance value implies a maximum load impedance, or minimum load current.
4) To obtain some gain at 100Hz, the final values of output inductance and capacitance and loop gain are chosen so that the d.c. loop gain is 1000 while maintaining unit gain at the resonant frequency of the output filter, that is at 2·6kHz.

Earthing

In designing and building the prototype power supply, it was found that earthing was very critical for ensuring stability, particularly when connecting various parts of the circuit together. Large currents, when switched at very high speeds even through relatively small inductances (such as a length of wire), can generate extremely large voltage transients. For a current of 10A switched in 100ns, a figure of 100V/μH or approximately 1V/cm of wire is typical. Therefore it is important that the paths round which these currents flow should be as short as possible. For this reason, a number of decoupling capacitors were used across the main supply lines. A small local decoupler was placed as close as possible across the output transistor and filter network, followed by a larger one which of necessity, was placed further away, and finally an even larger reservoir capacitor about 50 to 80mm distant. In this way, the small, preferably ceramic, capacitor, which is best able to deal with the most troublesome high-frequency components of the current, is nearest the source of the problem, while the electrolytics which in any case have some inherent inductance themselves, are suitably placed to deal with the lower frequency components. Care should be taken, however, to ensure that the smaller capacitors are able to deal with the large current spikes. Ideally, small ceramic capacitors are required having high frequency (100kHz) ripple current ratings of 1A or more.

The relative positioning of these components is shown diagrammatically in Fig. 23. The thickest lines indicate the connections which should be made with the shortest lead lengths. The connection of one section of the circuit to the next should also be made in such a way as to obtain optimum noise immunity. Each section should be referenced to the section into which it is driving (while avoiding earth loops), the exception being the feedback circuit which is driven from a current source.

Radiation

A certain amount of radiation is generated both by the filter inductance and the switching transistor itself. The screening of the prototype supply is indicated in Fig. 19 by the dashed line around the power stages. However, the problem of radiation was not considered in detail in the design of this circuit because the main aim was to study basic circuit principles. An article dealing exclusively with the problem of interference in switched-mode power supplies should be published later.

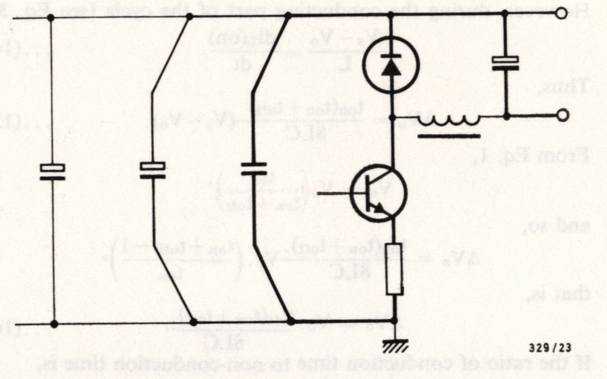

Fig. 23—Lead lengths (thickest lines should be shortest leads)

Isolation

With this power supply system no isolation exists between input and output voltages. However, if mains operation is necessary, a mains transformer may be used, as with conventional stabilizer systems.

APPENDIX 1

Calculation of Inductance and Capacitance Values

As shown in Fig. 6, the inductor current under normal operating conditions is a triangular waveform. When the inductor current is greater than that required by the load, the excess current charges the reservoir capacitor, thereby causing the voltage across it to rise. Similarly, when the inductor current is less than that required by the load, the excess current is supplied by the reservoir capacitor and the voltage across it falls. The charge flowing into the capacitor during one cycle is shown by the shaded area in Fig. 6.

$$\text{Area} = \tfrac{1}{2}\times\text{base}\times\text{height}.$$

Therefore,

$$\Delta q = \tfrac{1}{2}\times\left(\frac{t_{on}+t_{off}}{2}\right)\left(\frac{di_L(on)}{dt}\cdot\frac{t_{on}}{2}\right), \qquad \ldots(11)$$

where $\frac{di_L(on)}{dt}$ is the rate of increase of current during the conducting part of the cycle. (Note that $\frac{di_L(on)}{dt}$ and $\frac{di_L(off)}{dt}$ — the rate of decrease of current during the non-conducting part of the cycle—are only equal when the duty cycle is 50%). This increase in charge represents a voltage change across the capacitor of,

$$\Delta V_o = \frac{\Delta q}{C}, \qquad \ldots(12)$$

where ΔV_o is the peak-to-peak voltage ripple on the capacitor. This is because an equal voltage decrease occurs when the same amount of charge is removed from the capacitor. Thus, the total ripple voltage ΔV_o is given by:

$$\Delta V_o = \frac{\Delta q}{C} = \frac{t_{on}(t_{on}+t_{off})}{8C}.\frac{di_L(on)}{dt}. \qquad \ldots(13)$$

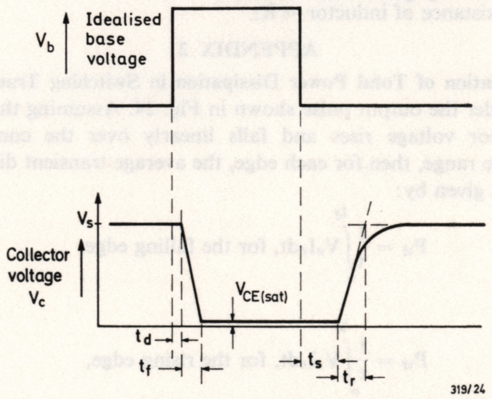

Fig. 24—Output pulse from switching transistor

However, during the conducting part of the cycle (see Eq. 3),

$$\frac{V_s-V_o}{L}=\frac{di_L(on)}{dt}. \qquad \ldots(14)$$

Thus,

$$\Delta V_o=\frac{t_{on}(t_{on}+t_{off})}{8LC}(V_s-V_o). \qquad \ldots(15)$$

From Eq. 1,

$$V_o=V_s\left(\frac{t_{on}}{t_{on}+t_{off}}\right),$$

and so,

$$\Delta V_o=\frac{t_{on}(t_{on}+t_{off})}{8LC}.V_o.\left(\frac{t_{on}+t_{off}}{t_{on}}-1\right),$$

that is,

$$\Delta V_o=V_o.\frac{t_{off}(t_{on}+t_{off})}{8LC}. \qquad \ldots(16)$$

If the ratio of conduction time to non-conduction time is,

$$\frac{t_{on}}{t_{off}}=\eta,$$

then,

$$t_{on}=\eta t_{off},$$

and,

$$t_{on}+t_{off}=\frac{1}{f}.$$

Therefore,

$$t_{off}=\frac{1}{f(\eta+1)}, \qquad \ldots(17)$$

and,

$$t_{on}=\frac{\eta}{f(\eta+1)}. \qquad \ldots(18)$$

From Eqs. 16, 17, and 18,

$$\frac{\Delta V_o}{V_o}=\frac{1}{8LCf^2(\eta+1)}. \qquad \ldots(19)$$

Thus, for a given output voltage and switching frequency, the ripple can be specified by the magnitudes of the filter inductance and capacitance.

For a given ripple and output voltage, there are minimum permissible values of L and C which ensure that current flows in the inductor throughout the cycle. This is shown by considering the end of the non-conducting part of the cycle when,

$$\frac{di_L(off)}{dt}.\frac{t_{off}}{2}+\frac{V_o}{R_L}=0, \qquad \ldots(20)$$

where R_L is the load resistance. Also, from Eq. 4,

$$\frac{di_L(off)}{dt}=-\frac{V_o}{L}.$$

Therefore, the critical (minimum) inductance is,

$$L_c=t_{off}\,\frac{R_L}{2},$$

or

$$L_c=\frac{R_L}{2f(\eta+1)}. \qquad \ldots(21)$$

Similarly, for a given output ripple voltage, the critical capacitance is, from Eq. 19.

$$C_c=\frac{V_o}{8L_cf^2(1+\eta)\Delta V_o}. \qquad \ldots(22)$$

Note that these expressions are based on the following assumptions:

1) Switching times $\ll t_{on}$ and t_{off}
2) C has negligible series resistance
3) Resistance of inductor $\ll R_L$

APPENDIX 2

Calculation of Total Power Dissipation in Switching Transistor

Consider the output pulse shown in Fig. 24. Assuming that the collector voltage rises and falls linearly over the complete voltage range, then for each edge, the average transient dissipation is given by:

$$P_{tf}=\frac{1}{\tau}\int_o^{t_f}V_cI_cdt, \text{ for the falling edge,}$$

and

$$P_{tr}=\frac{1}{\tau}\int_o^{t_r}V_cI_cdt, \text{ for the rising edge,}$$

where τ is the period of one complete cycle and the zero (reference) time is taken to be the start of the switching edge in each case. Thus, for the falling edge,

$$P_{tf}=\frac{1}{\tau}\int_o^{t_f}V_cI_cdt, \qquad \ldots(23)$$

where

$$V_c=V_s\left(\frac{t_f-t}{t_f}\right), \qquad \ldots(24)$$

because at $t=0$, $V_c=V_s$ and at $t=t_f$, $V_c=0$.

Similarly,

$$I_c=I_m\frac{t}{t_f}, \qquad \ldots(25)$$

because at $t=0$, $I_c=0$, and at $t=t_f$, $I_c=I_m$.

Therefore,

$$P_{tf}=\frac{1}{\tau}\int_o^{t_f}V_sI_m\frac{(t_f-t)}{t_f^2}t\ ,$$

$$=\frac{V_sI_m}{\tau}\int_o^{t_f}\left(\frac{t}{t_f}.dt\right)-\frac{V_sI_m}{\tau}\int_o^{t_f}\left(\frac{t^2}{t_f^2}dt\right).$$

Therefore,

$$P_{tf}=\frac{V_sI_m}{\tau}\left[\frac{t^2}{2t_f}-\frac{t^3}{3t_f^2}\right]_o^{t_f},$$

$$=\frac{V_sI_m}{\tau}\left(\frac{t_f}{2}-0-\frac{t_f}{3}+0\right).$$

Therefore,

$$P_{tf}=\frac{V_sI_mt_f}{6\tau}. \qquad \ldots(26)$$

Similarly, for the rising edge,

$$P_{tr}=\frac{V_sI_mt_r}{6\tau}. \qquad \ldots(27)$$

Thus, combining Eqs. 26 and 27 gives the average transient power dissipation over one complete cycle $P_{t(av)}$ as,

$$P_{t(av)}=\frac{V_sI_m}{6}\left(\frac{t_r+t_f}{\tau}\right). \qquad \ldots(28)$$

As the switching frequency f_s is given by:

$$f_s=\frac{1}{\tau}$$

then,

$$P_{t(av)}=\frac{V_sI_m}{6}(t_r+t_f)\,f_s, \qquad \ldots(29)$$

or

$$P_{t(av)}\propto f_s.$$

The maximum dissipation due to $V_{CE(sat)}$ and the collector current is given by:

$$P_{s(av)}=V_{CE(sat)}I_m\frac{t_{on}}{\tau},$$

or

$$P_{s(av)}=V_{CE(sat)}I_mt_{on}f_s. \qquad \ldots(30)$$

Thus, adding Eqs. 29 and 30, the total dissipation in the device averaged over one cycle $P_{tot(av)}$ is:

$$P_{tot(av)}=I_mf_s\left[\frac{V_s(t_r+t_f)}{6}+V_{CE(sat)}t_{on}\right]. \qquad \ldots(31)$$

APPENDIX 3

Construction of Output Choke

Details of the construction of the output choke, L_4 in Fig. 19a, are as follows.

Core:	45mm ferroxcube pot core, type FX2243
Former:	DT2206
Spacer:	0·75mm
Winding:	10 windings of 26 turns, 0·5mm enamelled copper, wound in parallel (10-filar).